Single-Phase Grid Connected Inverter with DC Link Voltage Modulation

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Contents

Summary

Nowadays, the African continent is considered as a market with a lot of investment opportunities and it is characterized by prosperity and growing development. However, there is a serious corresponding sustainable energy need. The origin of this phenomenon is that the middle class in Africa, had a remarkable increase during a couple of decades ago. Moreover, people moved to the big cities. Consequently, more daily basic needs become on high demand. Most of them are food, clean water, infrastructure and energy. Developed countries such as China and European countries have started to invest in energy sector in Africa. So, the need is not limited to the other parts of the world where there is a strong tendency towards clean and affordable energy. The renewable energy sources are a key solution towards a substantial reduction of greenhouse gas emissions. The Sub-Saharan Africa has shown a high rate of use of wood for cooking and a lower number of people who have access to electricity. This has impact on the deforestation and the CO_2 emission increases due not only on the cooking activity but also on transport of the wood. Many woods must be imported from neighboring countries, that import needs fuel for trucks and increases traffic. The exploitation of the solar energy can reduce the use of wood. This will affect the indoor air quality for people using the solar energy while cooking. Indeed, the indoor air quality is under discussion,

while using charcoal or wood for cooking. The rate of access to electricity has increased a lot, but consequently it should be followed up with the use of renewable energy. This is especially needed in Rwanda. Many manufacturers from all over the world have made the PV (photovoltaic) modules affordable, as a lot of investments, research and development have been done to achieve it. However, the total cost of a PV system includes also the cost of the inverter, the cost of installing and grid connection. The grid connection cost, and installation cost are mainly depending on the local labor cost. The part of cost of ownership of the inverter becomes higher than the PV panels themselves due to the cost of the inverter combined with a typical lifetime of 10-12 years. This lifetime can be even less in tropical areas. Rwanda as well as in the other parts of the World experience a photovoltaic revolution in grid and stand-alone systems. Some countries use open land for the PV. Rwanda with small land and high population density should use the house roofs in order to save land and protect the vegetation. This aspect is somewhat comparable with Flanders.

From the present research side, it is good to investigate if other inverter topologies and control strategies might have an advantage. This might give indeed opportunities, but in the meantime, almost the whole problem setting of grid-connected inverters is understood. If, for grid tied PV inverters, a longer life could be combined with a lower or equal cost, it will reduce the total cost of ownership. One could look at the possibilities in choice of topology, components and the necessary control to achieve this. Today most of inverters using classical topologies, contain many electrolytic capacitors. By changing the topology and gate drives, one could reduce the number of electrolytic capacitors to only one, at a less critical place. Most inverter designers use electrolytic capacitors in many places as they were just used to do so. However, this “habit” reduces the lifetime of the inverter. This is not the only lifetime limiting element. They are other elements such as automotive grade processors, contact corrosion protection, and lightening protection. Of course, a “good engineering” also remains a key element for a longer life design for an inverter. The present work aims at developing a single-phase grid-connected inverter without an electrolytic capacitor at DC-link. The following objectives have been targets of the PhD work:

- Propose an inverter topology that can withstand the harsh working environment in Rwanda: use less electrolytic capacitors and a design where an electrolytic capacitor can be easily replaced;
- Study the stability of the topology;
- A gate driver of IGBTs without electrolytic capacitors;
- An adapted control of the inverter is needed.

The thesis has eight chapters. The first chapter is an introductory part. It shows the situation of the use of the PV system as renewable energy source in Rwanda. It discusses the source of CO_2 emission and the effect of using renewable energy on reducing it. It shows social and environmental impacts of integrating PV systems into traditional electrical network. The chapter also shows the parameters that can be based on in order to calculate the cost ownership of a PV system. The second chapter gives a literature review of a classical single-phase topology. It discusses different parts of a single-phase grid-connected inverter. It shows the different PWM schemes that are used for the single-phase inverter. It is in this chapter that the state of art is deeply identified. The third chapter proposes a topology that is based on a design of an inverter using a topology that replaces an electrolytic capacitor in DC-link by a much smaller polypropylene capacitor in the DC-link. It shows the benefit of using the polypropylene capacitors instead of electrolytic capacitors. The proposed topology can use a standard three-phase transistor bridge for a single-phase grid connected inverter. The bridge is used in a different way for single-phase injection with one leg for boost and two legs for an H-bridge. It is in this chapter that a DC voltage modulation technique is analyzed. Moreover, the calculation of RMS currents for the proposed topology compared to the classical topology is presented in this chapter. Chapter 4 analyses the stability of the DC-link of the proposed topology, partly using numerical inverse Laplace transform. The stability is not granted due to an inherent resonance of the topology. The validation of the stability was done by simulation as well as by a lab experiment. The fifth chapter proposes frequency synchronization using a Double Integration Method (DIM) after a brief discussion about drawbacks of the typical phase locked loop (PPL) control for single-phase inverters. The chapter presents some simulation, and lab results related to the DIM. The sixth chapter presents a design of an IGBT gate driver. It proposes a circuit with desaturation protection using the undervoltage protection of the gate driver. This chapter presents the simulation and lab results of the designed IGBT gate driver. The seventh chapter focuses on testing the whole system. In this chapter, the system was connected to the grid to test the inductor current control. Chapter 8 draws some conclusions and recommendations for the future work.

Samenvatting

Tegenwoordig wordt het Afrikaanse continent beschouwd als een markt met veel investeringsmogelijkheden en wordt het gekenmerkt door een sterke ontwikkeling en een meer welvaart. Parallel is er echter een behoefte aan duurzame energie. De oorsprong van dit fenomeen is dat de middenklasse in Afrika, opmerkelijk is toegenomen enkele decennia geleden. Bovendien verhuizen de mensen naar de grote steden. Aldus wordt de vraag ook groter naar dagelijkse basisbehoeften. Dit zijn vooral voedsel, zuiver water, infrastructuur en energie. Landen zoals China en de Europese landen zijn begonnen te investeren in de energiesector in Afrika. De behoefte aan hernieuwbare energie is dus niet beperkt tot andere delen van de wereld waar men streeft naar een duurzame en betaalbare energie. De hernieuwbare energiebronnen zijn een belangrijke middel om de uitstoot van broeikasgassen terug te dringen. Het Afrika ten zuiden van de Sahara heeft ook nog een groot percentage van de bevolking dat hout gebruikt bij het koken en een beperkt deel dat toegang heeft tot elektriciteit. Het gebruik van zonne-energie kan het gebruik van hout verminderen. Inderdaad, de kwaliteit van de binnenlucht is een probleem, bij koken op hout of houtskool. Er is reeds te veel bos verdwenen en er moet veel worden geïmporteerd uit buurlanden, die import heeft

brandstof nodig voor vrachtwagens en verhoogt ook de verkeersdrukte. De behoefte aan elektriciteit is fors toegenomen, maar de integratie van hernieuwbare energie moet gelijke tred houden. Dat is vooral nodig in Rwanda. De wereldproductie ervan heeft de PV (fotovoltaïsche) modules betaalbaar gemaakt, waarbij er veel investeringen in onderzoek en ontwikkeling werden gedaan om dit te bereiken. De totale kosten van een PV-systeem omvatten echter ook de kosten van de omvormer, de kosten van de installatie en de netkoppeling. De kosten voor de netkoppeling en de installatiekosten zijn vooral afhankelijk van de lokale arbeidskosten. De levenscycluskosten van de omvormer worden nu hoger dan de PV-panelen zelf. Dit omdat de kosten van de omvormer enkele keren moet vervangen worden, omdat deze een typische levensduur heeft van 10-12 jaar, soms ook zelfs minder in tropische gebieden. Zowel Rwanda als andere delen van de wereld ondergaan een fotovoltaïsche revolutie in netgekoppelde en onafhankelijke systemen. Sommige landen gebruiken het open veld voor de PV. Rwanda met een hoge bevolkingsdichtheid zou vooral daken moeten gebruiken om grond te sparen en de vegetatie te beschermen. Dit aspect is enigszins vergelijkbaar met Vlaanderen.

Vanuit het huidige onderzoek gezien, is het goed om na te gaan of andere inverter topologieën en controlestrategieën een voordeel kunnen hebben. Dit kan inderdaad opportuniteiten opleveren, maar ondertussen wordt bijna de hele probleemstelling van netgekoppelde omvormers begrepen. Als de netgekoppelde PV-omvormers een langere levensduur bereiken met een lagere of gelijke kost, dan zouden de levenscyclus kosten dalen. Men kan de mogelijkheden in de keuze van de topologie, componenten en de nodige controle onderzoeken om dit te bereiken.

Heden gebruiken de meeste omvormers met een klassieke topologie, een groot aantal elektrolytische condensatoren. Door het veranderen van de topologie en de gate sturingen, kan men het aantal elektrolytische condensatoren te beperken tot slechts één, en dan nog op een minder kritische plaats. Meestal gebruiken de ontwerpers van invertoren immers veel elektrolytische condensatoren, louter "uit gewoonte". Die "gewoonte" vermindert echter de levensduur van de omvormer. Dit is echter niet het enige levenslange beperkende element. Er zijn ook andere verbeteringen mogelijk zoals "automotive grade" processors, corrosiebescherming van contacten, en bescherming tegen bliksem. Uiteraard is ook een "goed vakmanschap" nodig bij het ontwerp voor een langere levensduur. Het huidig werk is gericht op het ontwikkelen van een kosteneffectieve omzetter voor netkoppeling aan een éénfasig net met een hogere betrouwbaarheid. De volgende doelstellingenzijn de elementen van het doctoraat:

- Een inverter topologie voor die de omgevingsinvloeden in Rwanda kan weerstaan: minder elektrolytische condensatoren en een ontwerp waar die elektrolytische condensator kan vervangen worden.
- Studie van de stabiliteit van de topologie.
- Een gate driver voor IGBTs zonder elektrolytische condensatoren.
- Een aangepaste controle van de omvormer is nodig.

Het proefschrift heeft acht hoofdstukken. Het eerste hoofdstuk is een inleidende deel. Het omvat de situatie van het gebruik van het PV-systeem als hernieuwbare energiebron in Rwanda. Het bespreekt de oorsprong van de CO2-uitstoot en het effect van het gebruik van hernieuwbare energie op het terugdringen ervan. Het toont de maatschappelijke en milieueffecten van het integreren van PV-systemen in een traditioneel elektrisch netwerk. Het hoofdstuk toont ook de parameters om de levenscyclus kosten van een PV-systeem te berekenen. Het tweede hoofdstuk geeft een literatuuronderzoek van een klassieke eenfasige topologie. Het bespreekt verschillende delen van een éénfasige netgekoppelde invertor. Het toont de verschillende PWM-algoritmes die worden gebruikt voor een éénfasige omvormer. In dit hoofdstuk wordt de stand van de techniek nader besproken. Het derde hoofdstuk stelt een topologie voor waarbij de elektrolytische condensator in DC-verbinding door een veel kleinere polypropyleen condensator wordt vervangen. Het illustreert het voordeel van het gebruik van de polypropyleen condensatoren in plaats van elektrolytische condensatoren. De voorgestelde topologie kan een standaard driefasige transistorbrug gebruiken voor een éénfasige aangesloten netomvormer. De brug wordt dan op een andere manier gebruikt voor éénfasige injectie, met één been voor een spanningsverhogende hakker en twee benen voor een H-brug. In dit hoofdstuk wordt een gelijkspanningsmodulatie techniek geanalyseerd. Ook wordt de berekening van de effectiefwaarde van de stroom voor de voorgestelde topologie in vergelijking met de klassieke topologie in dit hoofdstuk voorgesteld. Hoofdstuk 4 analyseert de stabiliteit van de DC-koppeling van de voorgestelde topologie, deels met behulp van een numerieke inverse Laplace-transformatie. De stabiliteit is niet evident door een inherente resonantie in de topologie. De validatie van de stabiliteit werd gedaan door simulatie en door een labo experiment. Het vijfde hoofdstuk stelt een frequentie synchronisatie voor met behulp van een dubbele integratiemethode (DIM) na een korte discussie over de nadelen van de typische fase vergrendeling lus (PLL) controle voor éénfasige omvormers. Het hoofdstuk presenteert een aantal simulatie en experimentele resultaten met betrekking tot de DIM. Het zesde hoofdstuk presenteert een ontwerp van een IGBT gatesturing. Het stelt een circuit met desaturatie beveiliging voor, gebaseerd op het gebruik van de onderspannigbescherming van het gate driver IC. Het hoofdstuk presenteert de simulatie- en praktische testen van de ontworpen IGBT Gate driver. Het zevende hoofdstuk is gericht op het testen van het hele systeem. Het is in dit hoofdstuk dat het systeem wordt aangesloten op het net en de stroomregeling in de smoorpoel getest wordt. Hoofdstuk 8 trekt enkele conclusies en aanbevelingen voor toekomstig werk.

List of abbreviations

C	Capacitor
CSI	Current Source Inverter
CCM	Continuous Conduction Mode
COPCC	Constant Off Time Peak Current Control
D	Diode
DC	Direct Current
DISM	Double Integration Synchronization Method
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FT	Fourier Transform
GHG	Greenhouse Gas Emissions
HF	High Frequency
HPF	High Pass Filter
IGBT	Insulated-Gate Bipolar Transistor
L	Inductance
LT	Laplace Transform
LTI	Linear Time-Invariant
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum power point tracking
OLG	Open Loop Transfer Function
PI	Proportional-Integral
PID	Proportional integral derivative

PLL	Phase Locked Loop
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
SIC	Silicon Carbide
SPWM	Sinusoidal Pulse width Modulation
SVM	Space Vector Modulation
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
UVLO	Under Voltage Lock Out
VCO	Voltage Controlled Oscillator
VSI	Voltage Source Inverter

List of Symbols

V_{OC}	Open circuit voltage
I_{SC}	Short circuit current
V_{ref}	Reference- voltage
I_{ref}	Reference current
$\delta_{\alpha 1}$	Duty ratio
E_{off}	The turn-off energy loss
i_{on}	Current at turn-on
i_{off}	Current at turn-off
V_{dc}	Instant value of the DC bus voltage
$V(t)$	Line-to-line voltage or phase voltage of grid.
V_{r}	Reference signal voltage
V_{c}	Carrier signal voltage
F_c	Carrier signal frequency
DISM	Double integral Synchronisation Method
f	Frequency
$\mathrm{F_s}$	Switching frequency
$\mathrm{I_d}$	Diode current
I_{rms}	Root mean square current
η	Power efficiency of the converter
A_r	Attenuation ratio
$V_{\mathrm{grid-peak}}$	Grid voltage peak

V_{grid}	Grid voltage
$\delta_{\max}$	Maximum duty ratio
I_{su}	Boost converter DC link current
$i_{\mathrm{b,avg}}$	Average current injected into the inverter
$I_{\mathrm{b,rms}}$	Root mean square current injected into the inverter
$T_{\mathrm{int\,k}}$	Time for interval k
$i_{\mathrm{int,k}}$	Current for interval k
$\delta_{\mathrm{int,k}}$	Duty ratio for interval k
δ_{peak}	Peak duty ratio
$i_{\ \mathrm{peak}}$	Peak current
Vg	Instantaneous voltage at grid side
ω	Angular frequency
$\omega_{\min}$	Minimal angular frequency
$\omega_{\max}$	Maximum angular frequency
R_G	Gate resistance
$R_{\mathrm{DS(on)}}$	Opto- coupler driver inductance
C_{GC}	Gate-collector
C_{GE}	Gate-emitter
V_{CE}	Collector-emitter
V_{CE}	Voltage between gate and collector
LCC	Lifetime Cycle Cost
RwF	Rwandan Franc
PoP/km^2	Population density per square km

List of figures

List of tables

Chapter 1

Introduction

Sub-Saharan Africa (SSA), considered as converging market investment opportunities and characterized by prosperity and development, is in a need of energy for more sustainable development. The origin of this phenomenon is that the middle class, in the SSA, has remarkable increased during a couple of decades ago [1]. Moreover, people have been moving to the big cities [1]. Consequently, more daily basic needs becomes on high demand. Most of them are food, clean water, infrastructure and energy. This influences the corresponding markets. Consequently, some developed countries such as China and European countries have started to invest in energy sector in the SSA [2]. Worldwide, the energy sector has started including and focusing on the renewable energy as clean and affordable energy. The most popular is the solar energy that is free and abundant, especially in the SSA. The solar energy has proven to have various applications in the human daily activities [3]. Rwanda, one of the Sub-Saharan African countries, tried to integrate the use of renewable energy in order to support the existing source of energy, to limit much use of wood as source of energy and to increase the percent of access of electricity [4][5] and to protect the environment and to reduce the CO_2 emission. The CO_2 emission has been a big challenge worldwide. Different countries tried to limit any source of energy that can increase the CO_2 emission [6]. A clear view of the toxicity of CO2 for breathing has been well defined for high concentration [7].

1.1 Trends of ppm from CO_2 emission and its effect

Many reports have discussed the trends of ppm from carbon dioxide emission. They pointed out some sources of CO_2 emission such as fossil-fuel combustion, flaring of waste gas during gas and oil production, cement clinker production and other limestone uses, feedstock and other non-energy uses of fuels, and several other small sources [8]. A various effects that humans can experience once they are exposed to high ppm from CO_2 are many. Yet, humans are not aware of the exact trends of ppm from CO_2 emission and its effect on health of people. Many papers have been showing the tendencies of CO_2 emissions and some monitoring systems of CO_2 emissions give the daily average part per million (PPM) value for CO_2 in atmosphere. Data in table 1 are given by two independent CO_2 monitoring systems (NOAA-ESRL and Scripps) based at the Mauna Loa Observatory in Hawaii. They are located at 3400 meters above sea level. It is obvious that CO2 emissions rise at a rate of 2.7 PPM per year. In terms of percentages, it increases 0.65% each year. In May 2019, the average value for carbon dioxide in the atmosphere was 415.7 ppm. After 81 years, in 2100, the CO_2 will be 621 ppm without considering the CO_2 from traffic and buildings. If 100 ppm from traffic and 100 from well-ventilated buildings are taken into consideration, in 2100, the carbon dioxide emission will be 821 ppm. Although humans and animals are able to deal with elevated levels of CO_2 in the short-term due to various compensation mechanisms in the body, the persistent effects of these mechanisms may have severe consequences in a perpetual environment of elevated CO_2. In other words, a lot of negative effects on human health exposed for long life to 821 ppm CO_2 can happen such as headaches, dizziness, fatigue, respiratory tract and short-term stress.

Table 1.1: Trends of ppm from CO_2 emission

DATE	**NOAA-ESRL (PPM)**	**SCRIPPS (PPM)**
MAY 15,2019	415.64	415.70
MAY 15,2018	412.50	412.60
MAY 15,2017	411.27	No data
APRIL 9 ,2016	No data	409.44
APRIL 13,2015	No data	404.84

Some anticipation must be done in order to avoid that tremendous increase in the carbon dioxide. Developing countries have to play a big role by using renewable energy sources by avoiding to pursue all traditional steps that developed countries went through starting by coal use for industries.

1.2 Energy and CO_2 emission limitation in Rwanda

Although Sub-Saharan Africa has many sources of energy, it has the least electrification rate globally [9]. Fig 1.1 shows evolution of fraction of population with electricity access in the SSA [4].

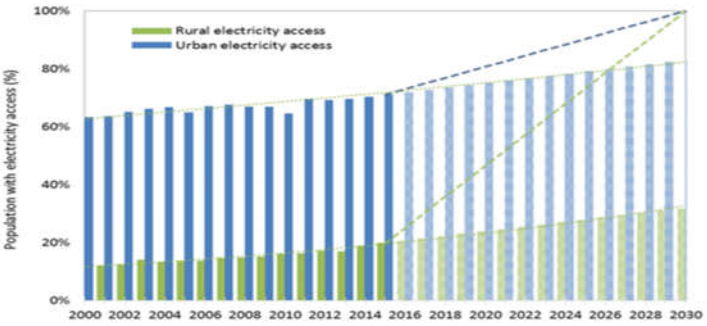


Figure 1.1: Evolution of fraction of population with electricity access in SSA [4]

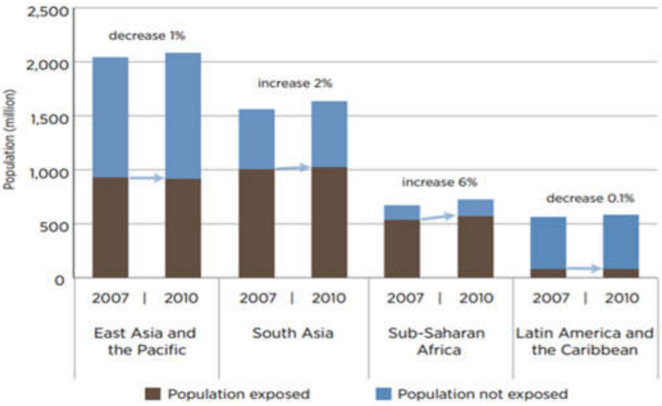


Figure 1.2: Population exposed to solid fuels use for cooking [10]

In rural areas, nearly 80% of population do not have access to electricity. The average residential electricity consumption per capita is 317 kWh per year and notably the least energy consumption rate per person in the world. Fig 1.2 compares the SSA to other countries in terms of population exposed to solid fuels use for cooking. It is obvious that the SSA population is still relying on solid fuels. In 2007, the region, with a population of 915 million people, has only 290 million of its citizenry having access to modern energy services. In 2010, it was a small positive change. People with access electricity was increased by 6%. Share of population relying on different types of cooking fuels in Sub-Saharan Africa in 2007 is shown in Fig. 1.3. In rural areas, 87% of the population used wood [11]. Two per cent had access to electricity. In urban areas, 30 % was still relying on wood. Some of the SSA countries have been working hard to overcome this challenge.

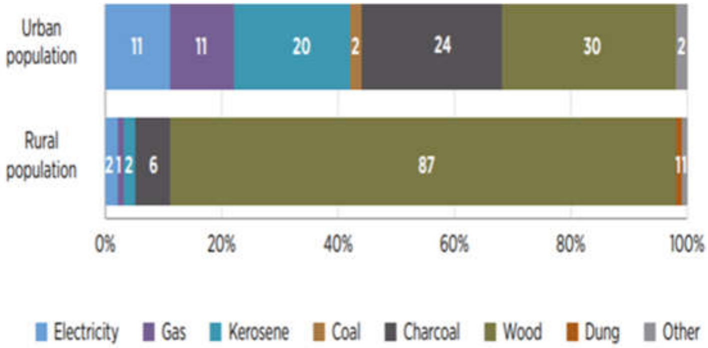


Figure 1.3: Different types of cooking fuels in Sub-Saharan Africa in 2007 [10]

The present work mainly focuses on Rwanda. Ten years back, Rwanda had 99 % of its population that was still using wood as source of energy. Moreover, importing petroleum as a source of energy consumed more than 40% of foreign exchange [12]. The government of Rwanda has been trying to limit the use of wood as long as it is inadequate and unhealthy for cooking, and promoted electricity.

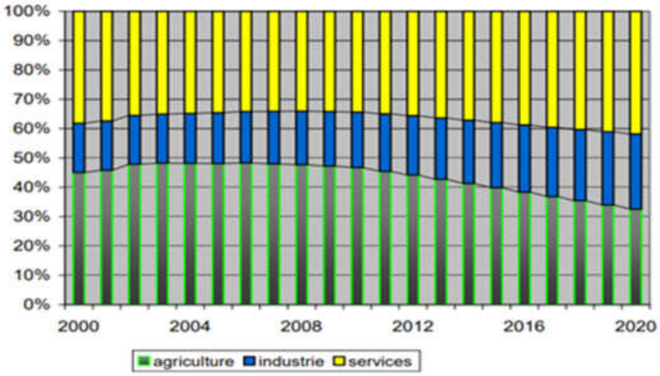


Figure 1.4: Transformation of Economic Activity 2000-2020 [12]

This has been helping the country to develop and to limit CO_2 emission. As a result, the environment is protected. Figure 1.4 shows the contribution of three majors sectors that are found in Rwanda. A big change was observed from 2008 up to 2019 where the industry services has increased from 15% to 35%. This results from the limit use of wood as source of energy. Consequently, the industry services have increased at the same time CO2 emission has be limited. The "vision 2020" plan has been targeting to reach at least 35 % of population connected to electricity and reduce the use of wood from 99% to 50%. Currently, the production of electricity is at a good step. Table 1.2 shows the production expectation. In this concept, the integration of renewable energy, on-grid and off-grid will dynamically help to achieve the Vision 2020 target.

Table 1.2: Access of electricity by "Rwanda vision 2020" projection [12]

YEAR	ACCESS (%)	INSTALLED CAPACITY(MW)	ENERGY (GWH)
2008	6	45	225
2010	11	85	353
2015	22	200	965.5
2017	28	300	1200
2020	32	400	1478

Even though the production is increasing, the cost of electricity per kWh is still high compared to Rwandan GDP per capita. Table 1.2 Vision 2020 vs. the New Electricity Supply Targets based on EDPRS, (Economic Development and Poverty Reduction Strategy) [12]. For residential use, the electricity tariff is set at a flat rate of 134 RwF per KWh (0.20 Euros/ kWh). Whereas for industrial customers are must pay 168 RwF per kWh (0.25 Euros /kWh) for high peak hours. During the intermediate, they are required to pay 96 RwF/KWh (0.14 Euros /kWh) for peak hours. Including more use of renewable source such as solar can reduce the cost of Electricity and limit CO_2 emissions.

1.3 Photovoltaic system in Rwanda

Based on the geographical location of Rwanda, the best candidate of renewable source is solar energy.

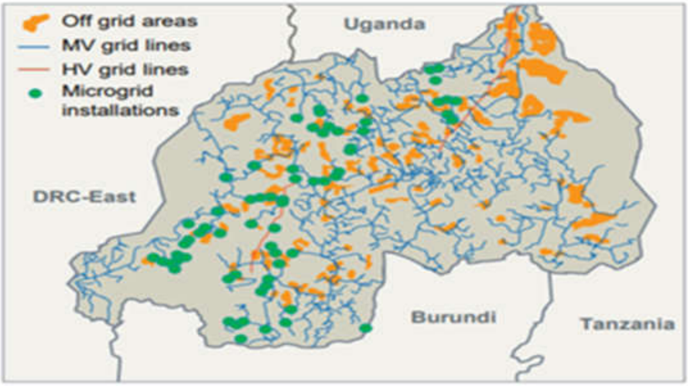
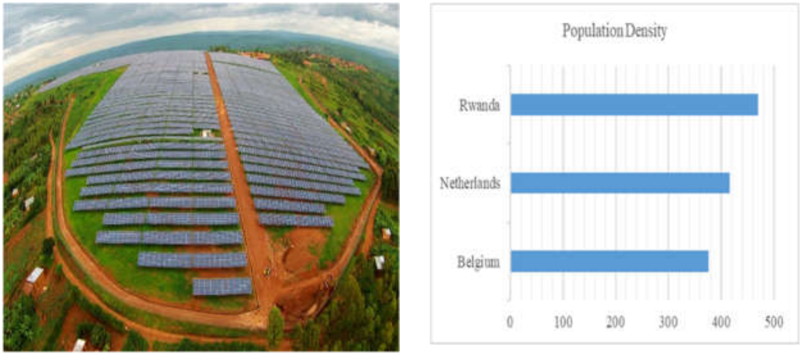


Figure 1.5: Current micro grid installations and designated off-grid areas in Rwanda [13].

The average daily global solar irradiation on the tilted surface is approximately 5.2 kWh/m^2 per day. This is because during both seasons, rainy and shiny, there is an abundant irradiation. There is a lot of possibility to install solar systems in Rwanda. The map in Fig. 1.5 shows the places planned for off grid and current connection (medium and high voltage transmission lines). Off-grid in yellow color and micro-grid in green color can help the rural areas to access to electricity. Many solar power project have been initiated and they have started operating. A 10 MW solar PV plant in the Kayonza Eastern Province was constructed. A 2.4 MW solar PV plant in south eastern Rwanda is operational. GigaWatt global has constructed 8.5 MW in Rwamagana (Figure 1.6) [14]. The solar power plant occupies 17-hectare. This is a good project. However, if the same projects are initiated with the same or higher power capacity, the land for vegetation will decrease considerably. Rwanda has high population density.



a) The 8.5 Megawatt (MW) power plant in Rwanda located in Rwamagana [14]

b) Rwanda population density (people/km^2) with a comparison to Belgium and the Netherlands [15]

Figure 1.6: PV use on land and Rwanda population density

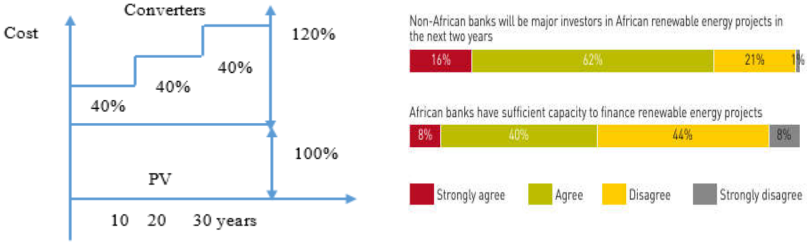
Having high population density, Rwanda is limited to use big land for the solar system. Fig. 1.6 b) shows that Rwanda has higher population density (470 people/km^2) compared to Belgium (376 people/km^2) and the Netherlands (417 people/km^2) [15]. The Netherlands and Belgium are leading in use of solar energy by exploiting the roofs of houses. Typically, in highly populated areas, with a lot of vegetation, PV would be rather on roofs than in separate farms that are in concurrency with agricultural land. Rwanda with small land can integrate the solar energy exploiting the roofs of houses. Solar energy can be made more economical by reducing investment and operating costs and by increasing the solar plant performance and the most significant cost reductions are likely to come from innovations in solar field design. The solar grid-connected systems without battery storage system can remarkably reduce the kWh cost once private sectors invest more in energy production. Many people can afford the production of electricity from solar energy.

1.4 Photovoltaic System reliability in Rwanda

A reliable Solar system can be defined as one that should be able to provide quality power to satisfy the system load with a reasonable assurance of quality and continuity of supply to its customers at all times. With the growth of the annually installed volume of grid-connected PV systems, there is a concern for the reliability of all PV system components, especially the PV inverter as a key component. In the other word, the lifetime of a PV inverter is influenced by various factors. Most of them are related to individual lifetime of the individual components. In practice, the PV inverter's lifetime is about 10 years [16]. This lifetime can be higher once some inverter electronic components with better reliability are used. The consumer strongly prefers to purchase a PV system where the components (i.e. inverter and panel) would have comparable expected lifetimes. Even though, at this moment there are no international standards for design qualification or type approval of inverters; at national levels various requirements on various aspects have to be met by inverters. For the Dutch normalization institute the Netherlands Energy Research Foundation (ECN) has developed a guideline for the design qualification and type approval for PV inverters [1]. The PV inverters are designed with consideration of their working environment. Many PV inverters imported from China or European countries to be used in Rwanda fail before their expected lifetime since their design qualifications do not consider the circumstances for which they are designed to operate. For instance in the Netherlands, small PV inverters (< 10 kWp) were mainly housed indoors under mild temperature and humidity conditions. The development of micro-inverters, AC modules where the small inverter is coupled directly to a single PV module and mounted on the rear side, introduces new operating conditions. At the back of a roof-integrated PV system, the temperatures range from well below zero Celsius up to 80 °C, with the entire range of humidity conditions. Under these conditions, the electronics must also be ready to operate for a period comparable to the expected lifetime of the PV module. The reason is that one has to mount on the roof to replace them. String inverters and the larger PV array inverters are available in special versions developed for housing in outdoor conditions. In Rwanda, it is very critical as lightning stroke frequently happen and have higher peak currents compared to non-tropical areas. This affects the inverter lifetime and the reliability of the inverter reduces. Many companies, Bbox and Mobisol provide inverters. The supplied inverters are not designed with consideration of the climate condition of Rwanda. Consequently, the inverter reliability is reduced.

1.5 Cost ownership calculation of a PV system

Solar energy technology is favourable for Sub-Saharan countries [17], however, a design of a Photovoltaic system requires a cost-effectiveness analysis so that the system can be competitive with other energy production technologies.



(a) (b)

Figure 1.7: PV investment: a) PV total cost of ownership cost period, b) Points of Views of sponsorships for renewable [18]

The optimization cost of a solar energy system starts from designing to servicing stages. Fig. 1.7 shows the point of view of sponsoring the PV and its period of total cost ownership. Eq. 1.1 found in [19] can be used to calculate the value of the total cost of the photovoltaic system (PV). This includes the PV panels plus inverter costs.

$$C_{PV}(X) = C_t(X) + M_t(X) \tag{1.1}$$

Where X is the optimization problem design variables. C_{pv}, C_t and M_t are the present cost of photovoltaic system, the manufacturing cost of the components of all system and maintenance cost, respectively.

The cost must be mainly calculated based on the PV panels, converters and servicing. The current cost of PV panels is 0.8 Euro/Wpeak VAT (value added taxes) included. Without including the VAT, the PV panel price is 0.7 Euro/Wpeak. Taking into account that the converter price can be 40% of the PV panel price, the total price of the PV system is 1 Euro/Wpeak. The transportation, installation and maintenance can be 40% of the total cost. The total cost of the PV is estimated at 1.3 Euros/Watt peak (1300 Euro/kWpeak) during 10 years [20]. In order words, the PV system price is 0.1 Euro/kWh. Comparing the solar price to current electricity price in Rwanda that is exploiting part of diesel power plants, the solar energy price might be cheaper. Considering the efficiency of diesel (40%) defined by lower heating value (LHV) and considering the current price of oil (0.6 Euros/liter), the price of electricity generated by diesel might be 0.15 Euros/kWh without including maintenance and installation fees. It is obvious that solar energy production can be cost effective compered to diesel engine energy production. Combining lifetime of the PV (30 years) [21] and of the converter in (10 years), the total cost of ownership period can be estimated Fig. 1.5 shows that the capital investment of the PV installation must include 100% of the PV panels for 30 years and 40% of PV panels each 10 years. The total benefit is estimated at 20% of the total investment. In Fig. 1.7, it is clear that the converters have to be replaced after each 10 years and the PV panels after 30 years. Eq. 1.2 and Eq. 1.3 give a picture of how the Lifetime Cycle Cost (LCC) of the PV system can be calculated.

$$LCC_1 = \sum_{\mathrm{i}=0}^{\mathrm{N}} \propto_{\mathrm{i}} K_i \tag{1.2}$$

$$LCC_2 = \sum_{\mathrm{j}=0}^{\mathrm{N}} \propto_{\mathrm{j}} K_j \tag{1.3}$$

Where K represents different costs (Total investment, capital replacement, maintenance, servicing), and α represents different factors which may affect the cost. LCC_1 and LCC_2 are respectively, the lifetime cycle cost for the PV panels and for the inverter. Eq. 1.2 and Eq. 1.3 are related. A company that would like to invest in PV system might consider both equation as well as the concept of Fig. 1.7.

1.6 Social and environmental impacts of integrating PV systems into traditional electrical network

There are still many diesel generators in Rwanda to locally support the electrical network [22]. Apart from the high operation costs of those generators, the PV systems, on grid or off grid, reduce substantially the greenhouse gas emission, other pollutants generated by the combustion engines. An author in [4] has showed a simple methodology for estimating the total amount of greenhouse gas emissions (GHG) once a PV system is integrated.

$$GHG_{\mathrm{old}} = E_{\mathrm{eng}}\,\mathrm{CO}_{2\,\mathrm{eng}} \tag{1.4}$$

$$GHG_{new} = \left((E_{\mathrm{eng}} - E_{\mathrm{enPV}})\,\mathrm{CO}_{2\,\mathrm{eng}}\right) + E_{\mathrm{enPV}}\,\mathrm{CO}_{2\,\mathrm{PV}} \tag{1.5}$$

$$GHG_{\mathrm{avoided}} = GHG_{\mathrm{old}} - GHG_{\mathrm{new}} \tag{1.6}$$

Where:

E_{eng} and E_{enPV} are energy provide by a diesel generator and a PV system respectively. CO_{2eng} represents an amount of CO_2 emissions from a diesel generator per kWh and CO_{2PV} is amount CO_2 emissions from a PV system per kWh. GHG_{old} is amount of CO_2 emissions of a diesel generator set installed to cover a specific electricity demand without a PV system. GHG_{new} is amount of CO_2 emissions of a generator set installed to cover a specific percentage of electricity demand once a PV system is integrated into a grid. Eq.1.6 , the difference between Eq.1.4 and Eq.15, expresses amount of CO_2 emissions that can be avoided while a PV system is integrated in order to support a diesel generator.

The case study was carried out for Sub-Saharan countries. The estimation was done based on the GHG emissions of a stand-alone diesel-generator set without a PV system.

Integrating the PV system, which can cover the same electricity demand as the diesel generator reduces the amount of GHG given by Eq. 1.6. This shows the impact of PV system installation on the environment. The other way is estimating the money, which can be saved once PV replaces cooking using charcoal. In the paper, Dawn of Solar cooking [23], it shown that a 400 Watt PV module coupled with 6.5 Ohm a cooking plate can cook rice for 3–4 people, twice in a day . In Rwanda, most of the time there is the sun at noon. Four small panels (250 watts per each) are enough for cooking. The cost of one panel is 120 €. Four panels cost 480 €. The lifetime of a PV is 30 years[21]. This means that the PV cooking system will cost 16 euro per year. A family of 3 people use 2 sacks of 25 kg for one months [23]. One sack costs 10 €. Hence, the family uses 20 € per month for cooking using charcoal. This is higher than what the family can spend using a PV cooking system.

1.7 Rationale and goals of the PhD work

The cost and reliability of the inverter is challenging as it is compared to the PV panels, that got cheaper and have a longer expected. PhD work aims at developing a single-phase grid-connected inverter without an electrolytic capacitor at DC-link. The objectives of the PhD work are:

- Propose an inverter topology that can withstand the harsh working environment in Rwanda;
- Study the stability of the topology;
- Propose gate driver of IGBTs of the inverter;
- Propose a control of the inverter.

During this PhD work, several reliability items were identified, but not all can be implemented in a single PhD research:

- use less electrolytic capacitors or design an inverter with electrolytic capacitor that can be easily replaced;
- use automotive grade components and processors that are designed and tested for a wide temperature and humidity range;
- Improve the protection so that an inverter can resist to indirect or direct lightning flashes.

1.8 Overview of the work done in this PhD thesis

The thesis has eight chapters. The first chapter is an introductory part. It shows the situation of the use of the PV system as renewable energy source in Rwanda. It discusses the source of CO2 emission and the effect of using renewable energy on reducing it. It shows social and environmental impacts of integrating PV systems into traditional electrical network. The chapter also shows the parameters that can be based on in order to calculate the cost owner ship of a PV system. The second chapter gives a literature review of a classical single-phase topology. It discusses different parts of a single-phase grid connected inverter. It shows the different PWM schemes that are used for the single-phase inverter. It is in this chapter that the state of art is deeply identified. The third chapter proposes a topology that is based on a design of an inverter using a topology that replaces an electrolytic capacitor in DC-link by a much smaller polypropylene capacitor in the DC-link. It shows the benefit of using the polypropylene capacitors instead of electrolytic capacitors. The proposed topology can use a standard three-phase transistor bridge for a single-phase grid connected inverter. The bridge is used in a different way for single-phase injection with one leg for boost and two legs leg for an H-bridge. It is in this chapter that a DC voltage modulation technique is analyzed. Moreover, the calculation of RMS currents for the proposed topology compared to the classical topology is presented in this chapter. Chapter 4 analyses the stability of the DC-link of the proposed topology, partly using numerical inverse Laplace transform. The stability is not granted due to an inherent resonance of the topology. The validation of the stability was done by simulation as well as by a lab experiment. The fifth chapter propose frequency synchronization using a Double Integration Method (DIM) after a brief discussion about drawbacks of the typical phase locked loop (PPL) control for single-phase inverters. The chapter presents some simulation and lab works related to the DIM. The sixth chapter presents a design of an IGBT gate driver. It proposes a circuit with desaturation protection using the undervoltage protection of the gate driver. The chapter presents the simulation and lab results of the designed IGBT gate driver. The seventh chapter focuses on testing the whole system. It is in this chapter that the system was connected to the grid and test the inductor current control. Chapter 8 draws some conclusions and recommendations for the future work.

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Chapter 2

Typical single-phase PV inverter topology

2.1 Introduction

The first chapter demonstrates that increasing the use of solar energy in different aspects off-grid and grid-connected will allow many people to have access to electricity. Nevertheless, this requires a lot of effort since different factors such as an inverter topology efficiency and PV panel prices must be look at in order to reduce the PV system cost [1][2]. In this chapter, an overview of the classical topology is given and it is compared with the proposed topology in chapter 3. The price of the PV panels is briefly discussed.

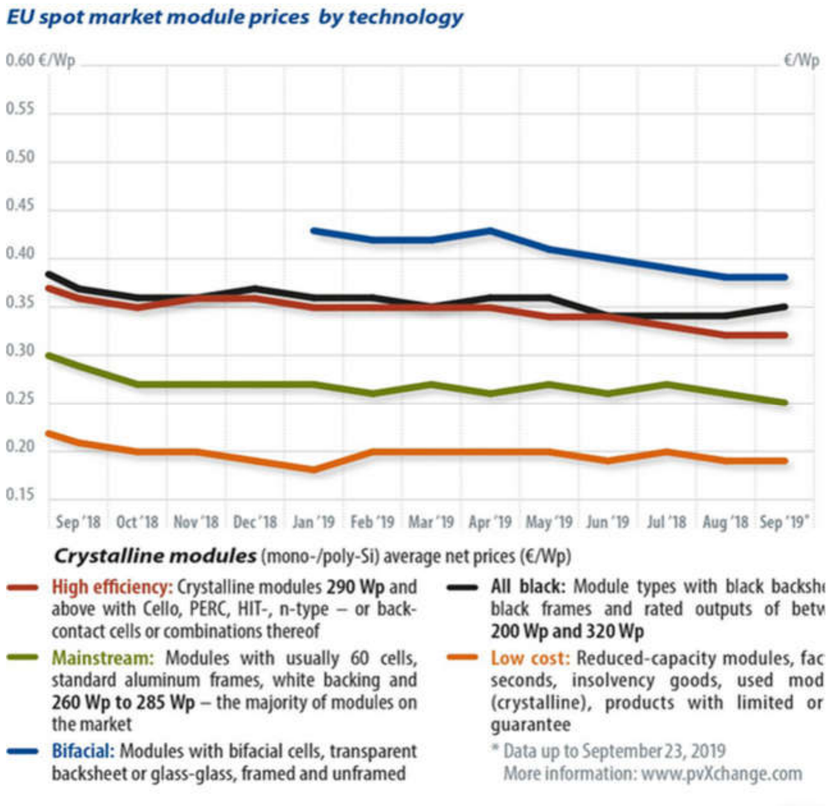

Figure 2.1: PV panels price reduction [3].

Today PV panels are expected to last at least about 25 years. The question will be about the cost and lifetime of the other components [4][2]. Figure 2.1 shows that the price of the PV panels has remarkably reduced. The issue of the cost remains at the level of the inverter The PV inverter reliability is one of the factors that cost wise affect the PV systems [5]. Based on its function, the PV inverter is a fragile part in PV systems. Hence, its lifetime of 10-12 year is low, compared to a PV panel lifetime of rather 25 years or more. This yields to quite high maintenance fees. As results, the Total Cost of Ownership (TCO) of a PV system is often higher than expected. Prospectively, enhancing the reliability of PV inverters can bring down the cost of PV energy. As listed in Chapter 1, for various types of PV inverters, one of the vital elements of the inverters that undesirably affect the inverter reliability performance are the electrolytic capacitors. The electrolytic capacitors have a limited lifetime by thermal ageing combined with voltage [6]. In warm countries such as Rwanda, the electrolytic capacitor lifetime can deeply affect the inverter reliability. Knowing the negative effect of the electrolytic capacitors in different PV inverter topologies leads at innovating new topologies with higher reliability. This is the same case for control electronic circuits and for the power stage. Replacing the electrolytic capacitors by another capacitor type of higher reliability and cheaper can have significant positive impact on the reliability of the PV inverter. This chapter shows the negative effect of the electrolytic capacitors based on a single-phase voltage source inverter (VSI) topology. The inverter is a full-bridge type.

2.2 A single-phase voltage source inverter (VSI) for PV applications

A voltage source inverter (VSI) topology is ubiquitous in the PV systems. The VSI topology can be a single phase or three-phase type. The single-phase topology is preferable for a residential PV system since the capacity is between 3-10 kW [7]. Fig. 2.2 shows the topology of a single-phase PV inverter. It is connected to a PV panel via a DC-DC boost converter. The boost converter is commonly used in the PV system to control the DC-link voltage [8].

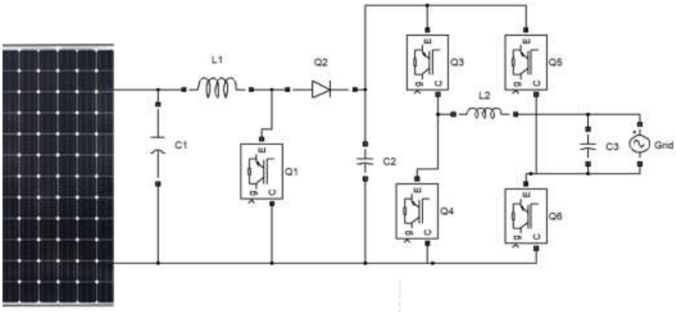

Figure 2.2: Single-phase full-bridge voltage source inverter (VSI) for PV applications

The inverter injects the power to the grid via a low-pass output filter. Several techniques can be used to control the switches of the topology in Fig. 2.2. The mostly used is the Pulse Width Modulation (PWM). Each part of the topology is discussed separately in the next sections.

2.2.1 DC-DC converter part

Most PV converters use DC-DC converters. The DC-DC converter topologies can be classified into two categories. Non-isolated DC-DC converters and isolated DC-DC converters. Non-Isolated converter, such as boost converter and quasi-double boost converter have been used for PV systems. These topologies are mainly used in the applications where the voltage step-up regulation ratio is low (usually less than 4) and usually they have higher efficiency than the isolated topologies because galvanic transformers that produce copper and iron losses are not used and less sum of peak current and voltage over the transistors. The inductor, L_1 and capacitor, C_2 in this circuit play a big role. During turn on period of Q1, the diode D1 is in reversed bias and electrical energy is stored in L_1. During turn off period, the stored energy in the inductor is transferred to C_2, which supplies energy to an H-bridge inverter made of two legs (Q4,Q3) and (Q6,Q5). This boost can work in two modes, conduction mode (CCM) and dis-conduction mode (DCM). In CCM, the current in L1 is greater than zero during turn off period. During DCM, the current in L1 drops to zero. This happens all the time at the end of each switching cycle. The PV panel array supplies the voltage to the boost converter and the boost converter sends the power to the inverter via C_2. To simplify the analysis of the boost converter, the inverter combined with the grid is replaced by an equivalent resistor R. The boost converter load. DC-DC converter can operate in one of two modes: CCM and DCM. The following paragraph presents the formulas for each case. The duty cycle formulas for CCM and DCM cases are respectively shown in Eq. 2.1 and in Eq. 2.2 [9]. Designing a converter requires to consider two operation modes. The state between them is called border mode. The current just reaches zero. Hence, the value of the inductor is given by Eq. 2.3.

$$D_{\mathrm{CCM}}(\mathrm{ideal}) = 1 - \frac{V_{\mathrm{PV}}}{V_{\mathrm{C2}}} \qquad (2.1)$$

$$\begin{aligned} D_{\mathrm{DCM}} \\ = \left(\frac{1}{V_{\mathrm{Pv}} \;\; - \dfrac{(V_{\mathrm{C2}} - V_{\mathrm{d1}}) * I_{\mathrm{Load}}}{V_{\mathrm{PV}}} * R_{\mathrm{eq}}} \right) \\ * \left(\sqrt{\frac{2\mathrm{L}_1 * (V_{\mathrm{C2}} + V_{\mathrm{d}} - V_{\mathrm{PV}})}{T_s} * I_{\mathrm{load}}} \right) \end{aligned} \qquad (2.2)$$

$$L_1 = \frac{V_{\mathrm{Pv}} * T_s}{2I_{\mathrm{LB}}} * D_{\mathrm{CCM}} * (1 - D_{\mathrm{CCM}}) \tag{2.3}$$

The current I_{LB} is the current at the border mode. Where D_{CCM} is duty cycle during Continuous Conduction Mode, D_{DCM} is duty cycle during Discontinuous Conduction Mode, $V_{\mathrm{pv,}}$ PV output voltage, V_{C2} Output voltage across C_2 (Fig. 2.2), V_{d}, Voltage drop in a diode of the switch Q_1, R_{eq} equivalent load resistor. Knowing the value of the inductor is not enough for optimizing the boost converter operation. Sizing effectively an output capacitor of the boost converter values the optimization of the boost converter. So far, many PV boost converters use the electrolytic capacitors at the DC link. The electrolytic capacitors have a maximum ripple current rating and the output capacitor of the boost converter is exposed to high ripple [10][11]. This is one of the reasons that there is high rate of failure of the electrolytic capacitors. Consequently, it affects the reliability of the PV inverter. To determine the required ripple rating of the output capacitor is to find the current in function of the RMS value of the current. The following formulas express the value of DC and AC components for the boost converter current.

$$I_{\mathrm{AC\,rms}} = \sqrt{\frac{\int_0^{\mathrm{T_s}} I^2(t).\,\mathrm{d}t}{T_s}} \tag{2.4}$$

$$I_{\mathrm{DC}} = \frac{\int_0^{\mathrm{T_s}} I(t).\,\mathrm{d}t}{T_s} \tag{2.5}$$

$$I_{\mathrm{rms}} = \sqrt{I_{\mathrm{DC}}^2 + I_{\mathrm{AC\,rms}}^2} \tag{2.6}$$

Where T_s is the switching period.

Eq. 2.4 and Eq. 2.5 show the RMS and DC component values of the capacitor current, respectively. Eq. 2.6 presents the relationship between the two values, RMS and DC component. In fact, the ac component of this goes into the capacitor while the DC component flows through the load.

The calculation of the boost converter passive components helps to optimize its functionality. In other words, the voltage at the DC-link must be kept constant. However, the PV output voltage is not constant. The Fig. 2.3 shows the boost converter characteristics while output voltage is maintained constant. Any voltage control strategy has to consider the boost converter behavior in Fig. 2.3. In order to optimize the voltage control the capacitor ripples must be minimized [12].

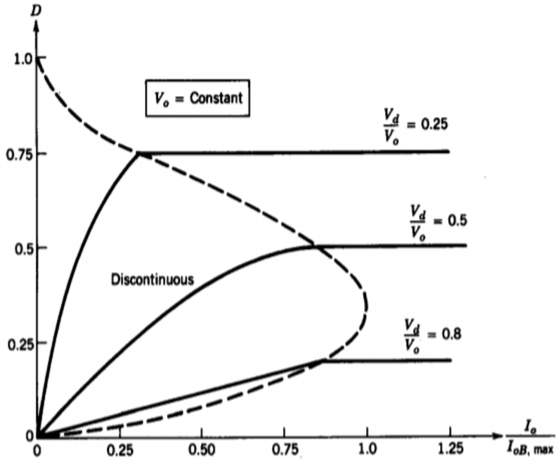

Figure 2.3: Boost converter characteristics with its output voltage constant [13]

Since the boost converter is a link between the PV inverter and the PV panel modules, it should take care of the Maximum Power Point Tracking (MPPT) control. Grid voltage and current control are necessary as well. The following section discusses the behavior of the inverter.

2.2.2 DC-AC converter part

The inverter in Fig. 2.2 is a single-phase inverter. The inverter is full bridge inverter with fours switches. Switches S_1 and S_2 are switched together while switches S_3 and S_4 are switched together alternately to S_1 and S_2 in a complementary manner.

In practice, a dead time is required to avoid the short circuit between two switches. The output load voltage alternates between $+V$d (from the PV panel) when S_1 and S_2 are ON and $-V$d (from the PV panel) when S_3 and S_4 are ON, irrespective of the direction of current flow. S_1 and S_2 are ON for a duration $0 \leq t \leq T_1$. Whereas S_3 and S_4 are ON for a duration $T_1 \leq t \leq T_2$. The instantaneous output power is given by 2.13.

$$P(t) = v(t)\, i(t) \tag{2.7}$$

$$V(t) = V\cos(\omega t) \text{ and } i(t) = I\cos(\omega t + \varphi) \tag{2.8}$$

$$P(t) = \frac{1}{2}VI\cos(\varphi) + \frac{1}{2}VI\cos(2\omega t + \varphi) \tag{2.9}$$

Where ω is the angular frequency of the ac system and, φ is the phase angle difference between the voltage and the current

The output power can be calculated based on Eq. 2.7 and Eq. 2.8. The fact that it is single phase results in a pulsating power of twice the frequency, if the output inductor and output capacitor do not store much energy, this pulsating power is delivered by the DC-link capacitor. As the PV system is grid connected, the topology in Fig. 2.2 faces much more challenges. It is clear that the power flow equation has two terms: the first term is a DC component whereas the second term is time varying at twice-fundamental frequency of the line. The second term is more about the ripple. VSI in Fig. 2.2 has a negative effect from this phenomenon. In fact, the low frequency reflect the voltage ripple on the DC-link. So far, it was only indicated that low frequency could cause the degradation of the inverter waveform quality. However, the low double grid frequency will force the inverter to use large-size passive components. Besides, the low frequency can be an origin of poor performance of the inverter [12]. Three types of RMS currents happen to appear in the DC-link capacitor: AC from the boost diode, DC power ripple, PWM switching ripple to the H-bridge. Subsequently, this can lead to the large-size passive components that are loss-full. In fact, the low frequency has an indirect negative effect on both cost and reliability of a PV system. The double frequency effect can be seen as well at the level of energy. Eq. 2.11 is deducted from Eq. 2.10. It gives the double-frequency energy provided by the DC-link. The simplified equation of the energy is found in Eq. 2.11.

$$\Delta E_g = -\int_0^{\mathrm{t}} \frac{1}{2} V_0 I \cos(2\omega t - \varphi)\mathrm{d}t \tag{2.10}$$

$$\Delta E_g = \frac{1}{2} C_{\mathrm{DC}}(V_{\mathrm{o-max}}^2 - V_{\mathrm{o-min}}^2) \tag{2.11}$$

$$C_{\mathrm{DC}} = \frac{\mathrm{S}_0}{\omega\ \Delta V_{\mathrm{DC}}\, V_{\mathrm{DC-av}}} \tag{2.12}$$

Where S_0 is an inverter apparent power, C_{DC} is the DC-link capacitance; V_{o_max} and V_{o_min} are desired maximum voltage and minimum voltage on the DC-link capacitor, the V_{o_min} is expected to be higher than the maximal grid voltage V_{DC} and $\Delta V_{DC,\ av}$ are voltage and ripple voltage on the DC-link respectively.

Eq. 2.12 shows the minimal capacitance required for the DC-link capacitor. The optimum design of a DC-link capacitor increases the performance of the PV system. In addition, it improves the reliability of the system. Yet, good sizing for the power stage of the PV inverter is not the only parameter to focus on. The following section gives a brief literature review on PWM modulation.

2.2.3 PWM modulation for a single phase inverter

The Pulse Width Modulated (PWM) scheme is mostly used for the power electronics circuits [14]. It offers the ability to change both the magnitude of the voltage and the frequency using a fixed DC voltage. There are various types of PWMs. Here, the literature review is more about the PWM in general. It shows both bipolar and unipolar PWM modulations schemes. Bipolar PWM uses a sinusoidal reference signal and a triangular carrier signal as in Fig. 2.4. When the instantaneous value of the sine reference is larger than the triangular carrier, the output is at $+V_{dc}$, and when the reference is less than the carrier, the output is at $-V_{dc}$.

$V_o = +V_{dc}$ for $V_{sine} > V_{tri}$;

$V_o = -V_{dc}$ for $V_{sine} < V_{tri}$;

The Switches in Fig. 2.2 will alternate as follows: Q3 and Q6 are on when $V_{sine} > V_{tri}$ ($V_o = +V_{dc}$) and Q5 and Q4 are on when $V_{sine} < V_{tri}$ ($V_o = -V_{dc}$) .

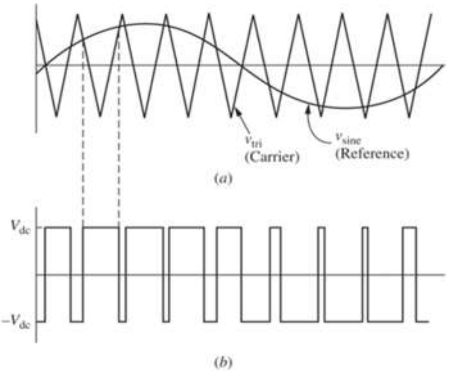

Figure 2.4: The bipolar PWM switching (using natural sampling) [15]

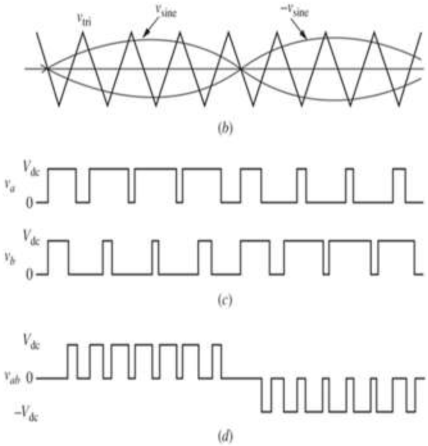

Figure 2.5: The unipolar PWM switching [16]

Unipolar PWM uses two sinusoidal reference signals and a triangular carrier signal to generate the switching pulses as in Fig. 2.5. The output is switched either from high to zero or from low to zero.

Referring to the topology in Fig. 2.2, the switching sequences are as follows:

Q3 is on when $V_{\mathrm{sine}} > V_{\mathrm{tri}}$;

Q6 is on when $-V_{\mathrm{sine}} < V_{\mathrm{tri}}$;

Q5 is on when $-V_{\mathrm{sine}} > V_{\mathrm{tri}}$;

Q4 is on when $V_{\mathrm{sine}} < V_{\mathrm{tri}}$;

2.2.4 Low-pass output filter part

For all H-bridge inverters, a low-pass output filter is obligatory to obtain the fundamental frequency output [17]. Generally, there are four different types of H-bridge inverter filters. They are L filter, LC filter, LCL filter, and LLCL filter. The topology in Fig. 2.2 has type LC filter. Therefore, this section focuses only on an LC filter. The LC filter is a second-order filter with an attenuation of -40 dB/dec . For designing an LC filter several factors must be taken into consideration [18]. The main factors are attenuation, cost and size of the passive components, the Comité International Spécial des Perturbations Radioélectriques (CISPR11) [19] can be used for the limit levels of the injected EMI in the grid. The trade-off of the design is that a higher capacitance can help to reduce the cost of the inductor. However, the system may encounter inrush current and high reactive current flow into the capacitor at the fundamental frequency. A lower inductance results in a higher capacitive current and high frequency current ripple, causing more no-load losses, resulting in a bad performance in cloudy and rainy moments. The performance of an LC filter varies from one application to another [20]. The resonance frequency of the filter becomes the grid impedance dependent for a PV inverter that is grid-connected type. For the stand-alone PV systems, the LC filter has high attenuation performance, but a rather high no-load loss. The author in [21], has showed that designing the LC filter does not only consider the output voltage but also concerns the reactive power: a big capacitor results in a capacitive no-load current. Hence, the following formulas can be employed. The PWM technique to control the inverter output voltage was considered during the LC filter sizing. Eq. 2.13 and Eq. 2.14 show the value of the capacitor and the inductor of the filter, respectively. In the two equations, it is obvious that the switching frequency is a key element that governs the sizing of an LC filter. In some books, the LC filter calculation is simplified. The effect of a type of the output voltage control of the PV inverter is not considered [21].

$$C_\mathrm{f} = K\frac{V_\mathrm{DC}}{L_\mathrm{f} f_\mathrm{s}^2 V_\mathrm{o,av}} \tag{2.13}$$

$$L_\mathrm{f} = \frac{V_\mathrm{o}}{I_\mathrm{o} f_\mathrm{s}}\left\{K\frac{V_\mathrm{DC}}{V_\mathrm{o,av}}\left[1 + 4\pi^2\left(\frac{f_\mathrm{r}}{f_\mathrm{s}}\right)^2 K\frac{V_\mathrm{DC}}{V_\mathrm{o,av}}\right]\right\}^{1/2} \tag{2.14}$$

$$K = \left[\frac{k^2 - \frac{15}{4}k^4 + \frac{64}{5\pi}k^5 - \frac{5}{4}k^6}{1440}\right]^{1/2} \tag{2.15}$$

Where $k = \sqrt{2}\frac{V_o}{V_\mathrm{DC}}$ with V_o and V_DC are inverter output and inverter DC-link voltages. $V_\mathrm{o,av}$ is average output voltage of the inverter. f_r is the fundamental output frequency and f_s is the switching frequency. I_o is the inverter output current.

However, it can be simplified if the voltage ripple at the output is neglected compared to the input voltage of the bridge.

2.2.5 A PV single phase Inverter control using a Phase Locked Loop (PLL)

Most PV inverters that are grid connected use a Phase Locked Loop (PLL) control. To design a PLL is a compromise. It becomes more complicated while the PLL must interface the PV inverter with a weak grid. This is due to the fact that there is frequency variation and harmonics distortions in the line voltages [22].

To synchronize the current to the grid voltage it is requisite to detect the variation of phase and frequency with grid voltage accurately and rapidly. PV integration to the grid causes many challenges to the traditional network. Thus, the implementation of PLL becomes not transparent for the user or the one that models it [23]. A large amount of penetration of distributed generation systems in the grid may give rise to the stability problem of the grid. In the chapter six of this book, it is shown that setting a current proportional to voltage does not work well with PLL. It creates a negative resistor in a wide frequency range because the circuit is not passive. Therefore, the way is to create a current set value that is not too much depending on the instantaneous voltage.

2.3 PV inverters in micro grid

The challenges discussed in the previous chapter have made researchers to come up with different types of PV inverters with different topologies and control architectures. According to the role of an inverter, the inverters that integrate a PV to an AC micro-grid have been classified into three groups: grid following (or feeding), grid forming and grid supporting [24].

Grid following inverters inject the active power generated by a PV source into the grid. These inverters operate at a unit power factor. In this type, a DC-DC converter is compulsory required to allow the MPPT implementation. The DC-DC executes the MPPT by modifying the operating point current or voltage of the PV generator [24]. These micro-generators are non-dispatchable types. To be capable to operate at a unitary factor and synchronize its output voltage to the grid, the following converters detect the grid frequency and its peaks. In fact, the inverters follow the grid behaviour in order to inject a sinusoidal current in phase with the grid voltage. It is rational for the inverters to need a voltage at the AC bus level as reference. Hence, they can follow that voltage for current synchronization. In this case, a current control is sufficient. The present types cannot be used for micro-grid with the energy storage devices (ESD) [24]. Consequently, another type, grid forming inverter type, can be used. The two main goals of the grid forming inverters are related to its two modes of operation. The first mode of operation is grid connected. The second mode of operation is islanded. During the first mode, grid-forming inverters regulate the active and reactive power injected to the AC bus to maintain the state of charge of the energy storage devices (ESD) and, in some cases, to improve the power quality. For the second mode, the grid forming inverters inject the sinusoidal voltage with regulated frequency and magnitude in the AC bus. In other words, the second goal of the forming inverters is to control the voltage source. In this case, the P-f/Q-V droop control is necessary. To achieve this a bidirectional DC-DC converter is used to interconnect the energy storage devices to the inverter. This aids to manage the charging and discharging cycles of the ESD. In some cases of the micro-grid characteristics, the main objectives of the following and forming inverters cannot be achieved. Henceforth, another type, grid-supporting inverter, is required. These inverters can be used either to support following inverters for grid-connected mode or to support the forming inverters. This chapter discusses the reliability of the first type, grid following inverter.

2.4 Conclusions

A voltage source inverter (VSI) topology is ubiquitous in the PV systems. The VSI topology can be a single phase or three-phase type. Most classical topologies use an electrolytic capacitor in the DC-link. The electrolytic capacitors do not tolerate high current ripples and the output capacitor of the boost converter is exposed to high current ripple. This is one of the reasons that there is high rate of failure of the electrolytic capacitors. The next chapter is focusing on the presented topology drawbacks and discusses on a proposed topology that can be used to implement an inverter that can cope with harsh environments.

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Chapter 3

Single-phase grid connected inverter with DC-link voltage modulation

3.1 Introduction

Now days, the PV modules are affordable, since a lot of investments, research and development have been done to achieve this. However, the grid connection and installation cost remains high [1][2]. The second chapter presents some drawbacks of a single-phase PV inverter topology that is commonly used. It showed the effect of the double frequency on the DC-link capacitor that could make the PV inverter use oversized passive components [3]. A price reduction of PV systems is possible through optimization of their converters. A change in the choice of components, topology and control can be considered to achieve a less-cost and effective PV inverter. This chapter proposes a topology that may reduce the cost and increase the performance of the PV inverter. The input voltage of the topology is related to a low number of panels for a typical household need. A typical 4-7 panel of 60 cells would already exceed the typical household needs. A 60-cell panel has a maximum power point voltage of about 30 V [4], so the input voltage of the topology would be significantly lower than the grid voltage.

3.2 Proposed topology for a single-phase grid connected Inverter

Figure 3.1 presents the proposed topology that can use a standard three-phase module for a single-phase grid connected inverter. The module is used in a different way for single-phase injection.

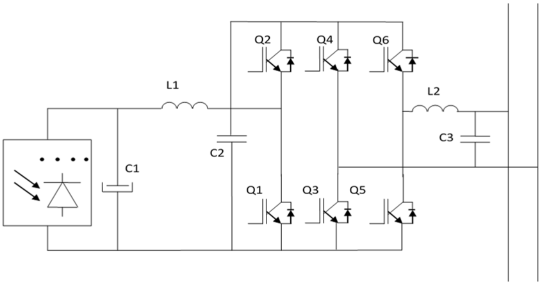


Figure 3.1: Single-phase PV converter using a three-phase bridge.

The presented topology has the input inductor L_1 and the output inductor, L_2. The advantage of using inductors at input and output is that low current ripples are obtained. PWM at the output H-bridge is only needed for low instantaneous voltages on C3. The capacitor C1 must be much larger in value and size than C2 to stabilize the PV voltage output. The voltage modulation is based on the topology in (Fig 3.2). Fig. 3.2 shows that the voltage on capacitor C2 is almost constant when the instantaneous grid voltage is low, and follows the grid when it is high Q3, Q4, Q5, and Q6 make a single phase H-bridge, whereas C3 and L2, form a low pass filter for EMC (Electromagnetic Compatibility). In the H-bridge, Q3 and Q4 are switched depending on the quadrant selection while Q5 and Q6 are switched depending on the quadrant and they are PWM modulated. This allows to use only one low pass inductor in the output. The proposed topology offers several advantages. The switching losses in Q1 are limited as the voltage across the C2 is lower than usual, and it switches only during some periods. The capacitor C2 has a lower value and it is a low loss type whereas the capacitor C1 is large. The switching losses in Q3 and Q4 are limited since they do not switch during the peak of the sine. The slow leg Q5-Q6 permits the use of use only one active filter inductor L2 to lower the EMI (radio interference) from the PV to grid. In this topology, the outer legs are better cooled than the mid-leg and can sustain slightly higher losses due to switching. The inductors L1 and L2 play a big role in the PV converter.

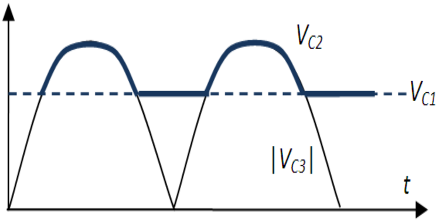


Figure 3.2: Control voltage across C2 capacitor.

The direct hard switching with high di/dt at the output level of the PV converter is reduced because of the presence of the inductors, and as switching occurs at a typically lower voltage. This makes the conversion smoother and with less EMC problems [5]. In addition, the losses in C2 are very low compared to electrolytic capacitors. However, the issue remains the controllability and the stability of the converter. This will be investigated in the next chapter. Fig. 3.3 shows the modulation mode control of the PV converter. The control function, *Fc*, generated by the feedback action is used to generate the six switches of the topology. The voltage at the output of the bridge is used to control the current in L2. The current control for the topology makes the system work in two modes. The way of control results in a multilevel action without being a multilevel converter topology.

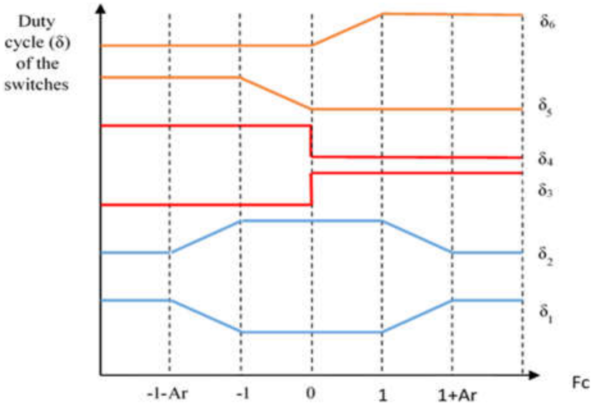
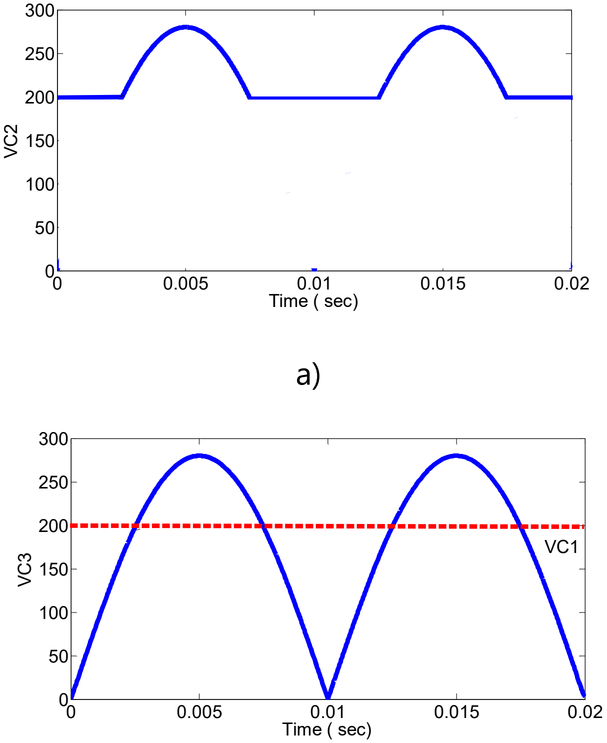


Figure 3.3: Modulation strategy for the transistors: depending on the saturation of duty ratios, other transistors are modulated by an attenuation ratio between gain for boost and gain for H-bridge, Ar.

3.2.1 DC-DC link interface of the proposed topology

The proposed topology has been developed based on the drawbacks of the topology discussed in chapter two. A parallel comparison of the DC-link RMS values between two topologies is established in the present chapter in order to illustrate the advantages of proposed topology. The first topology was upgraded by replacing a simple diode in boost converter by an IGBT, Q2. Moreover, the electrolytic capacitor is placed at the input of DC-DC converter. The propylene film capacitor is placed at the DC-link coupling between the boost converters and the inverter. To implement the DC voltage modulation using Fig. 3.2, Q2 is requisite. Q2 allows the bidirectional flow of power.



a)

b)

Figure 3.4: a) New topology DC voltage modulation and
b) PWM voltage modulation

The proposed topology with DC voltage modulation (Fig 3.4 a) has more advantages in terms of losses compared to the topology in chapter two. Fig. 3.4 b shows the voltage across DC capacitor. Some mathematical analysis are conducted based on grid voltage equation (Eq. 3.1) and duty ratio (Eq. 3.2.). Eq. 3.3 shows DC voltage RMS value at high frequency.

$$V_{\mathrm{grid}} = V_{\mathrm{p}} \cos(\omega t) \tag{3.1}$$

$$\delta = \cos(\omega t)\frac{V_{\mathrm{p}}}{V_{\mathrm{DC}}} \tag{3.2}$$

$$V_{\mathrm{rms-HF}}^{2} = V_{\mathrm{p}}^{2}(1-\delta)\delta \tag{3.3}$$

Where, δ is the duty cycle, V_{p} is peak value of the grid voltage, $V_{\mathrm{rms\text{-}HF}}$ is DC voltage RMS value at high frequency.

Putting Eq. 3.1 and Eq. 3.2 into Eq. 3.3, the DC voltage RMS value at high frequency becomes as follows:

$$V_{\mathrm{rms-HF}}^{2} = V_{p}^{2}(1-m\cos(\omega t))(m\cos(\omega t)) \tag{3.4}$$

$$m = \frac{V_{\mathrm{p}}}{V_{\mathrm{DC}}} \tag{3.5}$$

Fig. 3.4 shows that a zero value of $V_{\mathrm{rms\text{-}HF}}$ at DC-link occurs while the duty cycle equals one. For the topology, the DC voltage modulation helps to reduce the voltage RMS value. The following equation approximates the voltage RMS value at high frequency. The voltage RMS value at high frequency is in function of the DC-link voltage. Eq. 3.6 shows the relation between V_{Peak} and V_{DC}. Apart from the mentioned parameter, the Voltage RMS at high frequency depends on the mode of voltage modulation

$$V_{P} = V_{\mathrm{DC}} - V_{p}\cos(\omega t) \tag{3.6}$$

Connecting many PV systems at the distribution grid gives a big task to the utility companies for maintaining the grid stable [6][7]. Since the PV irradiation is naturally unstable, the PV grid connected converters operate at different operating points. Therefore, the DC-link power of a PV system must be stable for the different operating points. In the proposed topology, the boost converter mainly governs the voltage DC-link modulation. The more the boost converter is stable the more the topology is stable. The aim is to control the current in inductor L2 while switching Q1, so that the DC-link voltage follows the grid voltage during the top of the period and the bridge does not have to switch. It will not be an easy task as it has to be fast and stable.

3.2.2 Current RMS value of a DC-link capacitor

The current RMS value calculation takes into consideration two topologies. The classic topology A (Fig. 3.5) has the electrolytic capacitor at the output of the DC-DC converter and a small film capacitor at the input of the converter. The proposed topology B (Fig. 3.6) switches the placement of two capacitors in topology A. The electrolytic capacitor is at the input of the DC-DC converter and film capacitor at the output of the DC-DC converter. The usual DC-link electrolytic capacitor (type A) has to absorb current ripples from the boost converter, bridge and double frequency from the grid [8]. In the topology A, the electrolytic capacitor, C1 must withstand the overvoltage and the ripple current from the grid power [9]. The ripple from the step up and from the bridge plus the double frequency are highly reflected on the DC-link capacitor, that has more equivalent series resistance as it is an electrolytic [10],[11]. On the top, it receives some heat from the bridge, as it must be mounted very close to it, so the total temperature stress is higher. The topology type B, uses a small film capacitor in DC-link. As the previous, it has two main parts, a boost and an inverter.

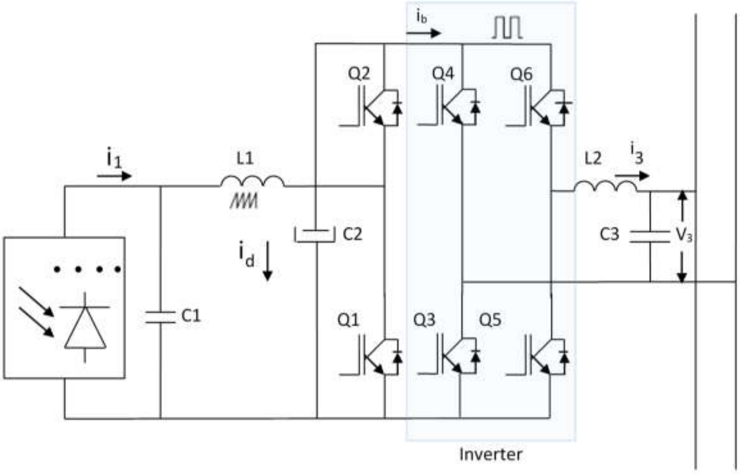


Figure 3.5: Topology type A

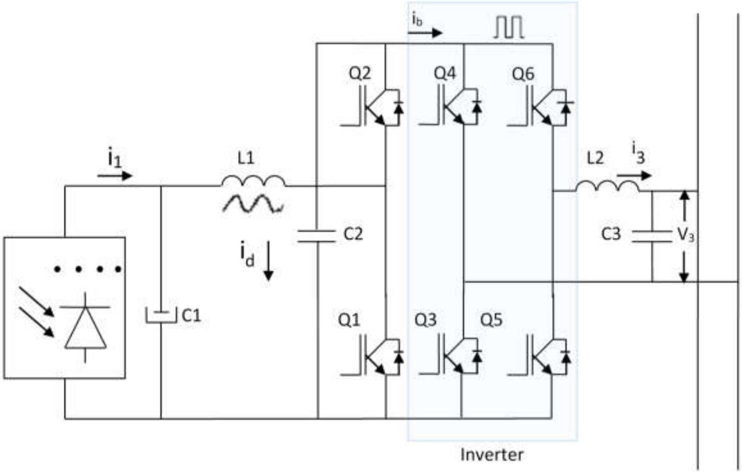


Figure 3.6: Topology type B

The 100 Hz storage for the pulsating grid power is now at the input. On top of the voltage, the current in L2 can be controlled while switching Q1 to make the grid current remain closer to the sine wave (Fig 3.4). Normally, a film capacitor in DC-link, as a solution, can tolerate the high frequency ripple and cannot absorb significant double frequency power ripple from the grid. This can be proven by current RMS calculation DC-link capacitors for both cases. There is a disadvantage that some ripple appears at the input voltage, but that can be used for maximum power point tracking. The fact that the electrolytic capacitor is at the input makes an advantage. It is easier to change it at the end of its lifespan. It can also absorb better a charge from indirect lightning. The whole converter could be built while using only one electrolytic capacitor. Also that capacitor can be eliminated, but additional losses can occur during higher voltages.

3.2.3 Calculation of current RMS value of capacitor in DC-link

There are many factors related to the DC-link capacitors that influence the performance of the PV converter [12]. The behavior of the current through the DC-link capacitor is among them. Henceforth, it is necessary to calculate the current RMS value of a DC-link capacitor of the inverter in order to know its performances [13][14].

$$\mathrm{Avg} = \frac{1}{\mathrm{b}-\mathrm{a}}\int_{\mathrm{a}}^{\mathrm{b}} i(t)\,\mathrm{d}t \tag{3.7}$$

$$\mathrm{RMS} = \sqrt{\frac{1}{\mathrm{b}-\mathrm{a}}\int_{\mathrm{a}}^{\mathrm{b}} [i(t)]^2\mathrm{d}t} \tag{3.8}$$

Where, *i(t)* is instantaneous current, a and b are time limits

In general, the definition of Average (Avg), and Root Mean Square Value (RMS) of a time varying function are respectively presented in Eq. 3.7 and Eq 3.8. However, depending on each topologies A and B, the current RMS of a DC-link topology can be different.

3.2.4 Calculation of current RMS value of capacitor in DC-link for topology A

The topology A has an electrolytic capacitor in the DC-link. Calculating the RMS current in DC-link capacitor in topology type A (Fig. 3.5) considers the electrolytic capacitor in the DC-link [15]. Eq. 3.9 shows that the current RMS of the C1 is a function of the RMS current from the step up and from the bridge converters assuming that the frequencies are not correlated. Eq. 3.10 shows the step up current RMS at high frequency.`

$$I_{\mathrm{c1,rms}}^{2} = I_{\mathrm{su,rms}}^{2} + I_{b,\mathrm{rms}}^{2} \tag{3.9}$$

$$I_{\mathrm{su,rms}}^{2} = (\,I_1(t))^2\,(1-\delta_1(t))\,(\delta_1(t)) \tag{3.10}$$

Where, $I_{\mathrm{b,rms}}$ is RMS of bridge current, I_{su} is DC-link current from Boost converter, and $\mathrm{i_{c,rms}}$ is the RMS current carried by the capacitor, C1. $I_1(t)$ is the current in inductor L1 and $\delta_1(t)$ is the constant duty ratio for Q1.

The high frequency RMS current component delivered to the bridge is calculated by Eq. 3.11.

$$I^2{}_{\mathrm{b,rms}}(\theta) = \frac{1}{\pi}\int_1^{\pi} \delta_{\max}\ \sin(\theta)\,(1 - \delta_{\max}\sin(\theta))(I_{\mathrm{L2max}}\ \sin(\theta))^2\,\mathrm{d}\theta \tag{3.11}$$

Where $\delta_{\max}$ is the maximum duty ratio for Q1 and, I_{L2max} is maximum current in L2. The RMS current in capacitor C2 considers as well the effect of double frequency from the grid power and the high frequency from the bridge plus step up converter [16][17]. Henceforward, the Eq. 3.12 is formulated.

$$I_{\mathrm{C1}}^2 = I_{100\ \mathrm{Hz}}^2 + I_{\mathrm{HF}}^2 \tag{3.14}$$

Where, $I_{\mathrm{HF}} = \sqrt{I_{\mathrm{su,HF}}^2 + I_{\mathrm{b,HF}}^2}$ is the high frequency RMS current component. The subscripts, su and b represent the step up and bridge converters respectively. $\mathrm{I}_{100\ \mathrm{Hz}}$ is 100 Hz current component from the grid power. Values for the passive components used to calculate the current RMS value for DC-link capacitor are shown in Table 3.1.

Table 3.1:Passive components for topology A

Components	**Types of components**	**Values**
Capacitor, C1	Polypropylene film	50 µF
Capacitor, C2	Electrolytic	2*2200 µF
Capacitor, C3	Polypropylene film	10 µF
Inductor, L1	Amorphous iron	700 µH
Inductor, L2	Amorphous iron	1400 µH

The calculation of RMS current in topology A considers 200V DC as input voltage of DC-DC converter. Current trough L1 is 15 A DC. $\delta_1(t)$ is 0.5. $I^2_{\mathrm{su,rms}}$ is 7.5 A. Combining Eq. 3.10 and 3.11, the current RMS in C2 at high frequency is evaluated, $I_{\mathrm{HF}} = 9.346\ \mathrm{A}$. The current R.M.S at double frequency, 100 Hz ripple, is 5.2 A. The total current RMS in C2 equals to 10.69 A. Here, $\delta_{\max} = 0.813$ and current in L2, $I_{\mathrm{L2max}} = 12.652\ \mathrm{A}$.

3.2.4.1 Calculation of current RMS value of capacitor in DC-link for topology B

Eq. 3.7 and Eq. 3.8 are still valid to calculate the current RMS value for the topology B and mathematical formulas in Eq. 3.15 and Eq. 3.16 can express them.

$$I_{\mathrm{b,avg}}(\theta) = \frac{1}{T_s}\left(\sum_k T_{\mathrm{int},k}\ i_{\mathrm{int},k}\right) = \sum_k \delta_{\mathrm{int},k}\ i_{\mathrm{int},k} \tag{3.15}$$

$$\begin{aligned} I_{\mathrm{b,rms}}(\theta) &= \sqrt{\frac{1}{T_s}\left(\sum_k T_{\mathrm{int},k}\ i^2{}_{\mathrm{int},k}\right)} \\ &= \sqrt{\sum_k \delta_{\mathrm{int},k}\ i^2{}_{\mathrm{int},k}} \end{aligned} \tag{3.16}$$

Where, $I_{\mathrm{b,avg}}(\theta)$ and $I_{\mathrm{b,rms}}(\theta)$ are respectively average and root mean square values of the current injected into the inverter. Both expressions are function of θ. $\frac{T_{\mathrm{int},k}}{T_s} = \delta_{\mathrm{int}\,k}$ are the interval duty cycles and $\mathrm{i}_{\mathrm{int},k}$ is the current for the interval *k*. Combining Eq. 3.15 and Eq. 3.16, the relation between the average and R.M.S current is shown in Eq. 3.17.

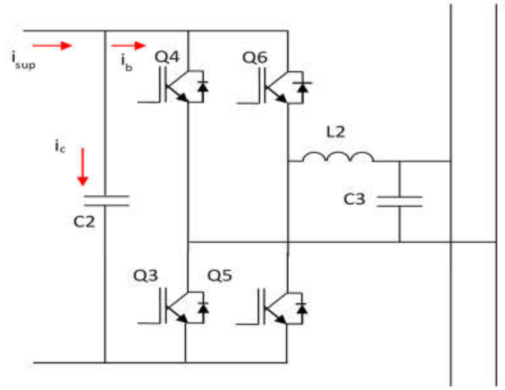


Figure 3.7: Current flows in the converter

$$I^2{}_{\mathrm{b,rms}}(\theta) = \; k_1\,.\,\delta_{\mathrm{peak}}.\,i^2{}_{\mathrm{peak}} \tag{3.17}$$

Where k_1 is a function of δ_{peak} and i_{peak} are the peak value of duty cycle and current of the bridge respectively. Considering Fig. 3.3, Eq. 3.16 can be written as a function of a sectorial δ.

The duty ratios δ_1 of the switches Q1 for boost converter, $\delta_{6,4}$ and $\delta_{5,3}$ respectively switch Q6,4 and Q5,3. Eq. 3.17 is, however, still valid once the switching period is considered. Taking into account the functionality of the topology B, the current flows are shown in Fig. 3.7. The step up current RMS can be expressed by Eq. 3.18.

$$I^2_{\mathrm{su,rms}} = \delta(1-\delta)\; I^2{}_{\mathrm{L1}} \tag{3.18}$$

Where, $I_{\mathrm{su,rms}}$ is R.M.S of bridge current, I_{L1} is DC-link current from Boost converter, and $I_{\mathrm{c2,rms}}$ is the RMS current carried by capacitor, C2.

Eq. 3.18 can be more developed based on Eq. 3.7 and Eq. 3.8. Hence, Eq. 3.19 and Eq. 3.20 can found as follows:

$$I_{\mathrm{su}}^2 = \mathrm{k}_2\, \delta_{\mathrm{peak}}\, i_{\mathrm{peak}} \tag{3.20}$$

$$I^2{}_{\mathrm{c2,rms}} = \mathrm{k}_1\, \delta_{\mathrm{peak}}\, i_{\mathrm{peak}} \tag{3.21}$$

Where, $\mathrm{k}_1 = \frac{1}{\pi}\int_0^{\pi} \sin^3(\theta)\mathrm{d}\theta$ and $\mathrm{k}_2 = \frac{1}{\pi}\int_0^{\pi} \sin^2(\theta)\mathrm{d}\theta$.

Eq. 3.20 and Eq. 3.21 are used for the practical values for the passive components for the topology B that are shown in Table 3.2.The input voltage and current are 200 V DC and 15 A DC, respectively. Fig. 3.8 shows the behavior of the current through C2 and it can be used to calculate the current RMS value of C2. This is the same as using Eq. 3.20 and Eq. 3.21. However, more figures showing the behavior of the current in the DC-DC converter and in the inverter can complement on calculating the current RMS value of the capacitor in DC-link.

Table 3.2: Passive components for topology B

Components	**Types of Components**	**Values**
Capacitor, C1	Electrolytic	3*2200 µF
Capacitor, C2	Polypropylene film	20 µF
Capacitor, C3	Polypropylene film	10 µF
Inductor, L1	Amorphous iron	700 µH
Inductor, L2	Amorphous iron	1400 µH

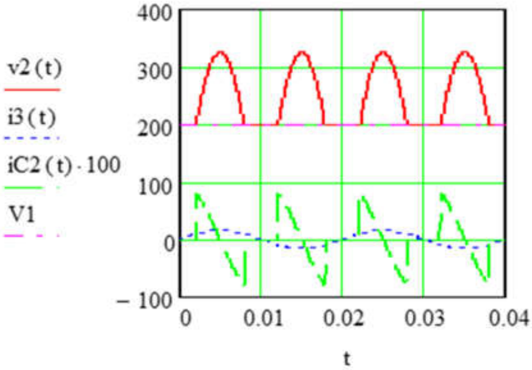


Figure 3.8: *ic2(t)* compared to *V1(t)*,*V2(t*) and *i3(t)*

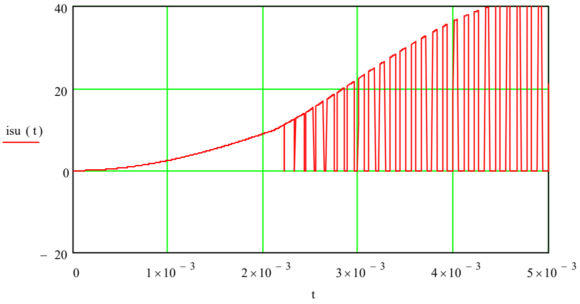


Figure 3.9: Current delivered by Boost Converter, i_{sup}

Figure 3.9 shows the current delivered by the step up converter. The current splits into two currents. One entering the bridge, i_b and another one passing through the C2.

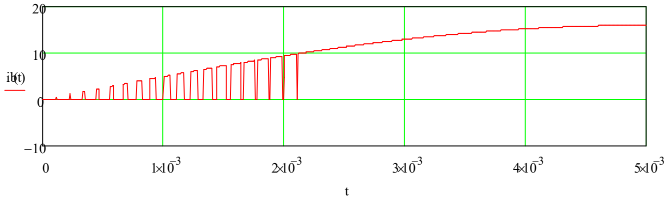


Figure 3.10: Current entering the bridge ,i_b with *L1*, and *L2* are infinite

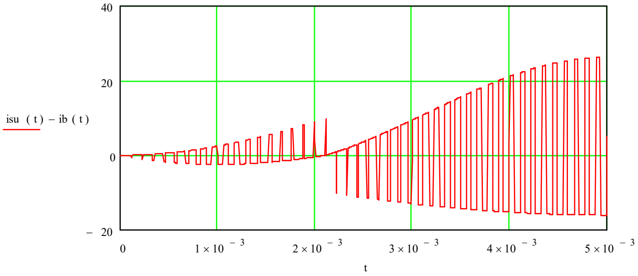


Figure 3.11: Current through the capacitor, *C2* with *L1*, and *L2* are infinite

Fig. 3.10 to Fig 3.13 shows the effect of inductor on current RMS values of the capacitor. Fig. 3.12 focuses particularly on the relationship between the duty ratio of the boost converter and current. The contributions of ripples in L1 and L2 are considered.

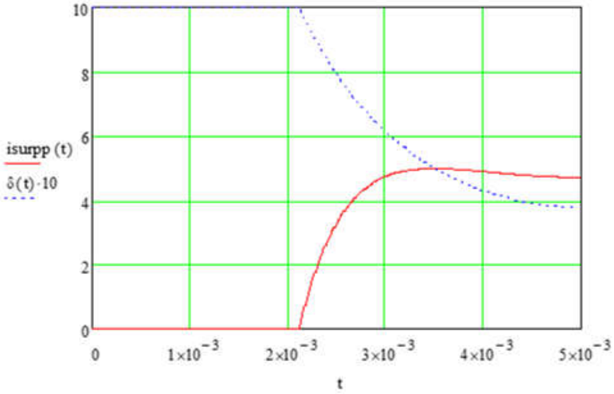


Figure 3.12: Boost converter current versus duty cycle with *L1*=600 µH and *L2*= 1400 µH

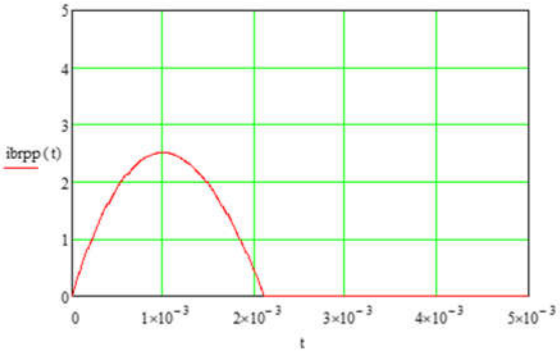


Figure 3.13: Peak to peak current in the bridge, with *L1*=600 µH and *L2*=1400 µH

Eq. 3.22 is formulated based on the Fig. 3.9 and the current RMS in C2 is calculated. It equals to 11.45 A.

$$I_{\mathrm{c2,rms}} = \sqrt{\frac{1}{0.005}\int_0^{0.005} ((i_{su}(t) - i_b(t))^2 \mathrm{d}t} = 11.45\ \mathrm{A} \qquad (3.22)$$

Eq. 3.23 and Fig. 3.11 are used to evaluate the ripple in step up converter issued by L1.

$$I_{\mathrm{supprms}} = \frac{2}{2\sqrt{3}} \sqrt{\frac{1}{0.005} \int_0^{0.005} \big(1 - \delta(t)\big)\, i^2{}_{su,pp}(t)\, \mathrm{d}t} \tag{3.23}$$

Based on the practical values of the two inductors on Fig. 3.12, the total RMS current in C2 can be recalculated using the following formula since the current ripples in L1 and L2 are orthogonal:

$$I_{\mathrm{c2,rms\,tot}} = \sqrt{I^2_{\mathrm{rms,L1,2}} + I^2_{\mathrm{supprms}} + I^2_{\mathrm{bpprms}}} = 11.534\ \mathrm{A} \tag{3.24}$$

Where, $I_{\mathrm{c2,rms\,tot}}$ is the total RMS current in C2, $I^2_{\mathrm{rms,L1,2}}$ RMS current ripple contributed by L1 and L2, I^2_{bpprms} is RMS current delivered to the bridge.

The previous equations cannot be used to calculate the value of the current at high frequency and at 100 Hz. Therefore, Eq. 3.23 can be exploited to calculate the contribution of double frequency on the RMS current in DC-link capacitor.

$$I_{100\ \mathrm{Hz}} = \frac{P\,\eta}{\sqrt{2}\, V\mathrm{g(t)}} \tag{3.25}$$

Where, P is the active power of inverter, η is efficiency of the converter at DC-link level, and $V\mathrm{g(t)}$ is instantaneous voltage at grid side. Based on the values in the Table 3.2, the $I_{100\ \mathrm{Hz}} = 11.534\ \mathrm{A}$. The RMS current at 100 Hz and at high frequency are respectively 10.45 A and 10.5 A.

In the common designs, the electrolytic capacitors are subjected to a large R.M.S current in the DC-link because they absorb the current ripple from the step-up converters and inverter [18]. Moreover, they are exposed to the double frequency from the grid. The heat of the bridge is transferred to them as well as the distance is short. Hence, the electrolytic capacitors are subjected to all problems at once. The film capacitor in the DC-link can be solution, where C1 becomes an electrolytic capacitor at the input level of the PV. Once C1 fails, the remainder of the inverter would be still protected. The start-up current is low as the electrolytic capacitor is charged by the PV cells and not by the grid. The replacement of C1 after 10 years is possible as it is placed at accessible level. There is a drawback that although the average current in Q1 is rather the same, rms and peak current in Q1 and L1 are bigger in B. This is the price to pay for lower capacitor losses. The inductor L1 is subjected to a higher peak current, but the inductor L2 becomes smaller while a smaller amount of HF voltage passes through it. In practice, in topology B, the core size of L1 and L2 can be the same, which is an advantage.

3.2.5 Matlab Simulation of the proposed topology

In order to verify the performance of the proposed topology, a computer-based simulation, Matlab 2013 has been used. The simulation illustrates the functionality of the DC voltage modulation strategy. The simulation is based on Fig. 3.6 that expresses the proposed topology. In addition, the simulation takes in consideration the feedback loop control shown on Fig. 3.14.a. The block diagram presents the measured inductor current, *IL2* compared to the current set value, Iref. In fact, the normalized (phase locked loop) is used to set up the current.

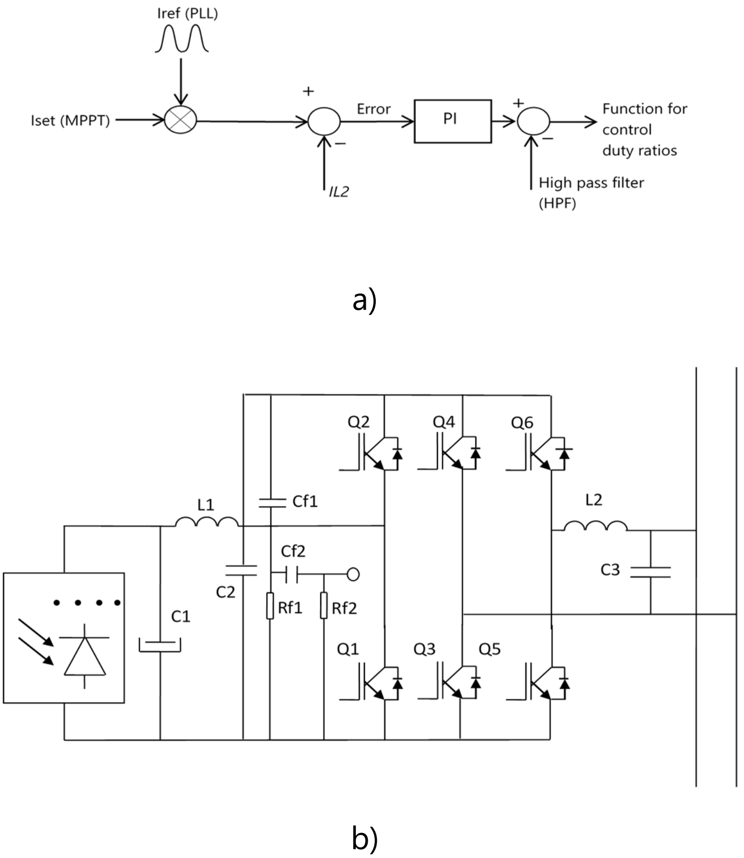


Figure 3.14: a) Control block diagram and b) Inverter

The error is controlled by the PI, which is mixed up with the effect of high pass filter (HPF) at the DC-link to generate the function to control the duty ratios, *FC*. The HPF effect is more discussed in fourth chapter and in [12].

3.2.5.1 Modulation strategy

The modulation strategy presented in Fig. 3.3 uses the same methods as PWM techniques. However, the challenge is how to control the current in inductor L2 for controlling both H-bridge and the boost converter. In fact, it concerns two different control modes, that have to be both stable, damped and follow well the set value and almost seamless cross-over. It seems that the same control topology can be used, but that the gain setting might be different. Therefore, the modulation has to consider the attenuation ratio, Ar, between the boost and the H-bridge duty ratios. The figure 3.3 has six segments. The three segments on left hand of zero are symmetric to three segments on the right side of zero. The left side is active once the grid voltage is lower than the DC voltage whereas the right side is active while the grid voltage is higher than the DC voltage.

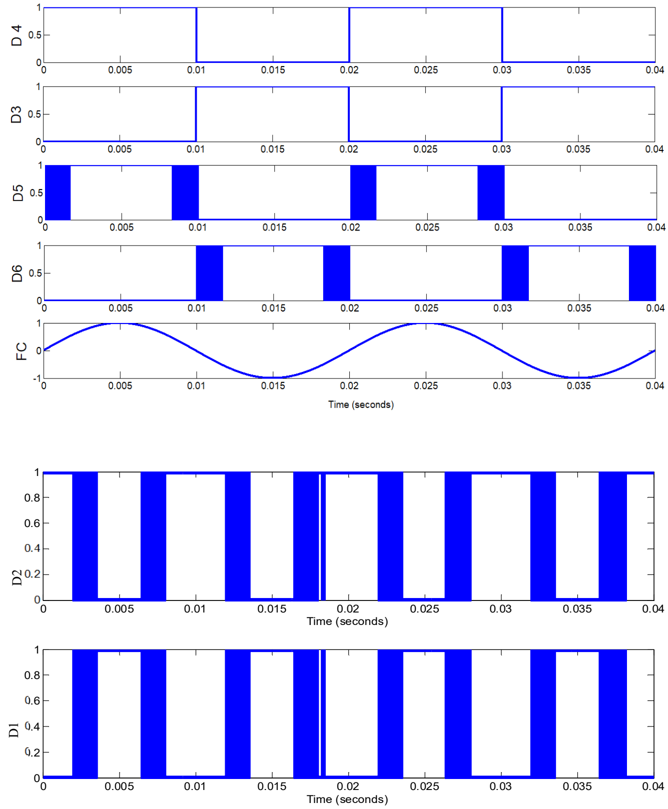
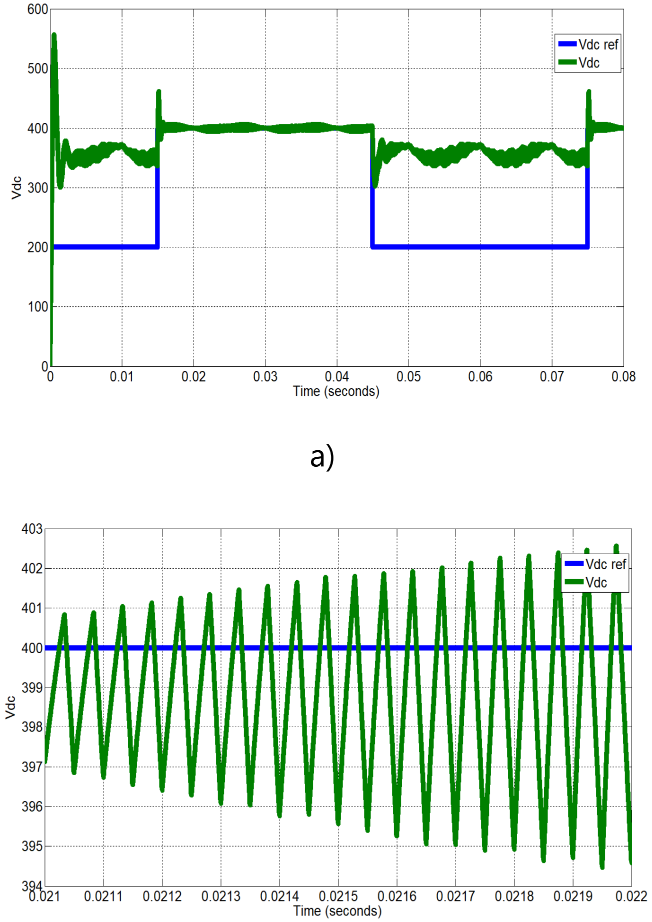


Figure 3.15: Behavior of 6 PWMs

In fact, they contain also two operating modes. The modulation must be able to switch from one mode to the other referring to the sign of the grid current in inductor L2. The current in the inductor is controlled referring to a reference value and it passes through the PI control that generates the controlling function, *Fc* (Fig. 3.3). The variation of the controlling function imposes the variation of the duty rations presented on Fig. 3.3. Ar, attenuation ratio between gain for boost and gain for H-bridge, is used to link the duty ratios of two DC-DC operation modes to an index modulation of the H-bridge inverter. Fig. 3.15 shows the behavior of the duty ratios related to the Fig. 3.3. To better analyze, DC levels that correspond to a boost converter or to H-bridge modulation operation are considered.

3.2.5.2 Two DC operation modes

This section shows the behavior of the grid while it is connected to the proposed single-phase inverter. On one hand, the simulation shows that the boost converter reacts while the DC voltage is greater than the grid voltage. This is considered as the first mode. This happens when the PV panel voltage output is less than 320 V DC. On the other hand, the simulation shows that the H-bridge reacts as buck converter while the DC-link voltage is greater than the grid voltage.



a)

b)

Figure 3.16: Voltage at DC-link :

a) Two operation modes, b) V_{DC} ripples

This is the second mode operation. Fig. 3.16 presents the two described scenarios. On Fig. 3.16, a, the voltage reference is set, V_{DC} ref. Its high value is 400 V DC and its low value is 200 V DC. The maximum set value illustrates the case the grid voltage is less than the DC voltage whereas the minimum set value presents the case the grid voltage is greater than the DC voltage. In case of the minimum value, the boost converter reacts. Duty ratios, δ_1 and δ_2 trigger Q1 and Q2 respectively as shown on Fig. 3.14. In case of the maximum value, Q2 is triggered low and Q1 is triggered high. Consequently, the boost converter is deactivated. The simulation shows as well the overshoot dynamics. At start up, the voltage overshoot is very high at the DC-link level. At the corner of the variation of the DC voltage set value the overshoot reduces. In fact, during the simulation, the DC voltage set value has big range of variation. However, in practice, the case of PV, the variation will be slow. Consequently, the observed overshoot behavior will be largely reduced. Fig. 3.17 shows the effect of the DC voltage variation superimposed in series with the inductor, whereas the effect on the current, *IL2* is shown in Fig.18.

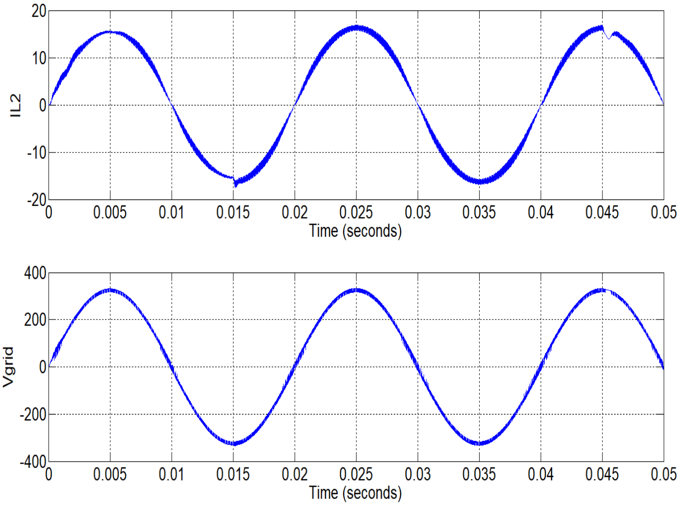


Figure 3.17: Grid voltage, *V*grid, and inductor current, *IL2* while DC-link voltage varies

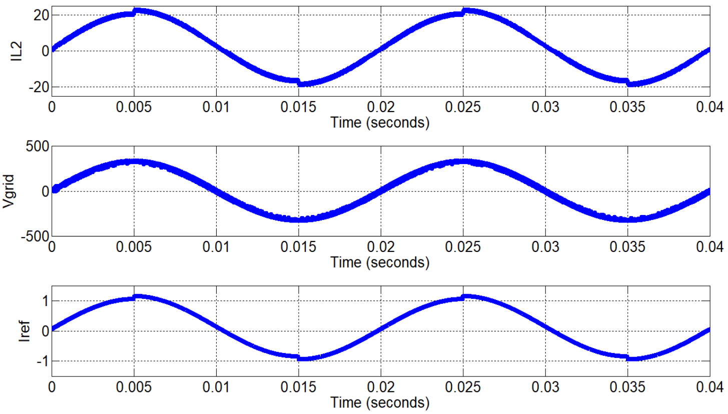


Figure 3.18: Grid voltage and inductor current,*IL2* with disturbance injection at grid level

The effect of the DC voltage variation is observed at 0.015 and 0.045 seconds. The control of the current dynamically follows the variation and it responds accordingly. Fig. 3.18 shows the behavior of the dynamics of the inductor current, *IL2* while the reference, I_{ref}, experiences the disturbances. The disturbances have been created on the top and the bottom of the I_{ref}. This helps to visualize the stability of the current control. In fact, the simulation targets to visualize the dynamism of the control of switches based on the control of inductor current, *IL2*. The simulation does not tends to show only the stability of the proposed topology. It presents the harmonics content of the topology that can be injected to the grid. The harmonics are compared to the IEEE standard harmonics. Fig. 3.19 shows the harmonics content of the inductor current. The Total Harmonics Distortion (THD) in the inductor current is 3.58%.

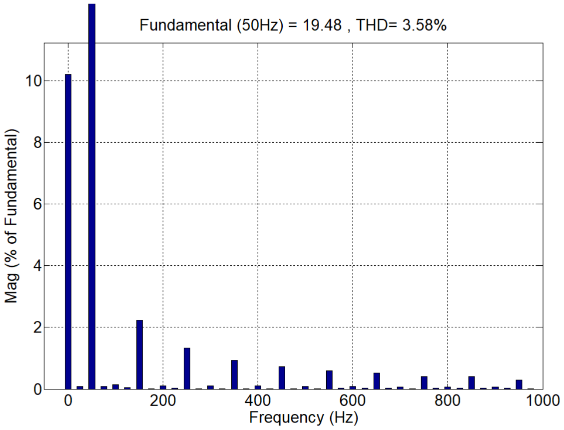


Figure 3.19: Inductor current, *IL2* harmonics contents

This complies with some standards. IEC standard 61727 stipulates that the THD for grid current should be lower than 5% [19]. On Fig. 3.19, the odd harmonics, 3rd to 9th are less than 3.5%. This complies with the mentioned standard. The standard specifies that odd harmonics from 3rd to 9th must be less than 4% [20]. In fact, a full topology contains an additional small inductor at the grid side and a parallel capacitor in between; this will attenuate the high frequency (radio frequencies), but not reduce the lower harmonics, so the conclusion is still valid in a qualitative way. No feedforward or learning corrections from one period to the next period have been used up to now; improvements of that kind could be still possible.

3.3 Conclusions

The proposed topology can use a standard three-phase module for a single-phase grid connected inverter. The inverter uses a specific voltage modulation. The middle leg plays a role of quadrant selection. The first leg is in charge of stepping up or down the voltage depending on the level of DC voltage. The inverter is low current ripple type since it has the input inductor L_1 and the output inductor, L_2. The advantage of using inductors at input and output combined with limited voltage levels is that low current ripples are obtained. Placing the electrolytic capacitor at the input and propylene film capacitors at DC-link reduces the current RMS value compared to the usual single-phase inverter. Consequently, the losses can be reduced. By Matalab simulation, the proposed topology presents a good performance in terms of stability. It has less harmonic injection. The next chapter focuses more on the stability analysis of DC-link of the proposed inverter.

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Chapter 4

Stability analysis of the DC-DC converter of the proposed topology

4.1 Introduction

Two types of controls are concerned for the proposed topology. A slow control for maximum power point tracking (MPPT) and a fast control for the AC current of the grid. The fast grid current waveform is challenging since a small DC-link capacitor is present in order to reduce the losses in the capacitors and the high frequency losses in the electrolytic capacitor.

4.2 MPPT control

The maximum power point control is a widely described problem [1], [2]. In the proposed topology, the ripple on the input capacitor can be used to tune the maximum power point. The electrolytic capacitor has to absorb the 100 Hz power flow of the pulsating grid power as shown on Fig. 4.1 [3],[4]. The ripple can be used to tune the MPPT. The maximum power point tracking (MPPT) can use the voltage ripple information, if the power at the highest voltage level is higher, then it has to move to a higher voltage, so the power can contain a 100 Hz ripple, where if the MPPT is attained, only a 200 Hz ripple in the power is observed. This type of problem is well known and can be solved within a few periods and it is not discussed in this chapter. The MPPT should not be too fast: it can cause fast grid fluctuations, but also a less known problem of arcing in switches when disconnecting a PV array can be observed.

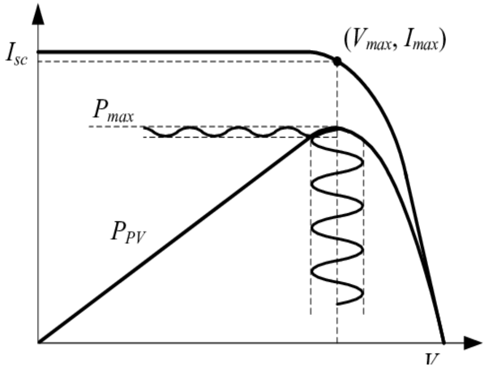


Figure 4.1: The low-frequency voltage ripple effect on maximum power point tracking [3],[4]

4.3 AC grid current control

The original problem setting is that electrolytic capacitors have a limited lifetime and quite high losses [5]. Film capacitors can carry much more RMS current and are smaller for a given high frequency current [6]. Moving the electrolytic capacitor in parallel to the PV array reduces its RMS current, has the advantage that it can be easier replaced, and helps to reduce the effect of a lightning stroke on the converter. Having a film capacitor at the DC-link has the advantage that it can be modulated, but it makes the stability of the AC current control challenging, for the right stability and harmonic content. Afterwards, the control has even two aspects: a modulation by the H-bridge or a modulation by the boost converter. Those controllers have to be joined in the right way to be able to have a seamless transient between them.

Henceforth, the stability analysis is necessary for the DC-DC converter. They are many techniques that can be employed to analyse the stability [7],[8]. Yet, this chapter use Numerical Inverse Laplace transform to investigate the stability of the system. The control does not consider only the converter components, but also it considers the physical process. In fact, its modelling includes an analogue to digital (A/D) conversion and time taken by timers to compare registers. This allows to have a continuous model.

4.4 Inverse Laplace Transform for DC-DC converters

The DC–DC converter operation is based on power electronics switches for the power conversion process.

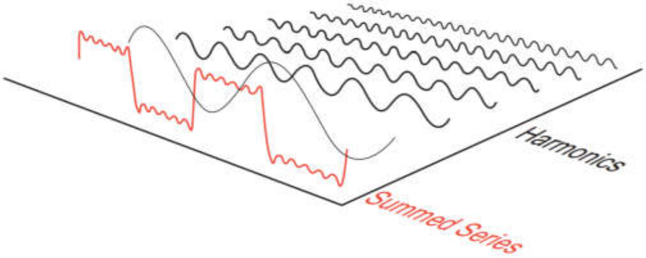


Figure 4.2: Graphical representation of the Fourier series of a square wave [9]

The sequential switching ON and OFF generates the voltage and current whose waves are periodic in some points of the circuit. This creates the nonlinearity in the DC-DC converters [10]. This limits the application of the concepts of stability, controllability, and observability, normally characterizing linear, time-invariant (LTI) systems to the DC-DC converter stability analysis [11],[12]. Different tools and techniques have been used to improve the stability analysis of the DC-DC converter. Laplace transform and related theories such as Fourier–series theory have been a good tool to analysis the stability of DC-DC converter. In fact, the Laplace transform is only valid after a sample and hold. If not, different inputs may give the same output. Fourrier transform modulates with (small) sine waves and can handle more difficult signals. A typical way to test the stability of a system is to apply a step or a square wave [13]. According to the Fourier-series theory, a good approximation of the sequential switching is to consider any periodic wave as a sum of sinusoids [14]. Henceforth, an arbitrary, periodic waveform, of any frequency, can be represented with great accuracy as a sum of sinusoids with variable amplitudes and distinct phase angles. Hence, to analyze the stability of a system based on Fourier is practical. Fig. 4.2 shows the Graphical representation of the Fourier series of a square wave. A drawback is that a very large number of harmonics are needed to reduce the ringing effect. Simulating a single step would need to apply a low-frequency square wave. Therefore, a numerical inverse Laplace transform algorithm can perform better. The numerical inverse Laplace transform algorithm has been used in analyzing the stability of different electrical circuits. The most popular are: Talbot, Week and Post's methods [15]. A strange effect is that an unstable system has a "stable" response, but reacts before the application of the applied step. So one recognises it as a non-causal response. But, the method has an advantage that one can gradually tune a system that is unstable with a first, not optimal set of parameters.

Based on a simple definition of Laplace transform, the present chapter develop an equation that is used to analyze the stability of a DC-DC converter.

Eq. 4.1 gives the definition of the unilateral Laplace that is mostly used [15],[16]. Bidirectional Laplace transform is equivalent to the unidirectional type if the poles and zeros are symmetrical [15], [16]. It is obvious that the Laplace Transform(LT) is a superset of the FT. The variable of LT is in the complex plane.

$$\mathcal{L}[f(t)] = F(p) = \int_0^{\infty} f(t)\, \mathrm{e}^{-pt} \mathrm{d}t \tag{4.1}$$

Where *f(t)* is a function with a real argument, *t*.

$F(p)$ is a function with a complex argument, $p = \sigma + \mathrm{j}\, 2\pi v$ with $(\sigma, v) \epsilon \mathbb{R}^2$ .Using a Fourier transform operator, Eq. 4.2 can be written as follows:

$$\mathcal{L}[f(t)] = F(\sigma + \mathrm{j}\, 2\pi v) = \int_0^{\infty} f(t)\, \mathrm{e}^{-\mathrm{j}\, 2\pi v t} \mathrm{d}t \tag{4.2}$$

Eq. 4.3 is a link between Fourier and Laplace Transforms. After some mathematical deduction, the inverse Laplace transform is expressed by the following equation:

$$\mathcal{L}^{-1}[\,F(p)] = f(t) = \int_0^{\infty} F(\sigma + \mathrm{j}\ 2\pi\nu)\mathrm{e}^{(\sigma+\mathrm{j}\ 2\pi\nu)t}\mathrm{d}\nu$$
$$= \frac{1}{2\mathrm{j}\pi}\int_{-\sigma}^{-\sigma+j\infty} F(p)\mathrm{e}^{pt}\mathrm{d}p \tag{4.3}$$

Eq. 4.4 is formulated by considering a frequency range between ω_{min} and ω_{max}, which are 0.01 rad/s and 100 Mrad/s respectively. This range should be sufficiently wider than the applied signal type.

$$f(t) = \frac{2}{2\pi}\int_{\omega min}^{\omega max}\left[\frac{\mathrm{e}^{(\sigma+\mathrm{j}\ \omega)\ t}}{(\sigma+\mathrm{j}\ \omega)}(F(\sigma+\mathrm{j}\ \omega))\right]\mathrm{d}\omega \tag{4.4}$$

Where ω=2πv, but the limits are converted to real values to have some meanings. The integral can also be replaced by a sum, with frequencies that are distributed in a logarithmic way:

$$f(t) = \frac{2}{j\ 2\pi}\sum_{m=0}^{n}\Big[\big(p(m+0.5) - p(m-0.5)\big)\ \frac{\mathrm{e}^{P(m)\ t}}{p(m)}(f(p(m))\Big] \tag{4.5}$$

Where: m and n are real numbers

$$p(m) = \sigma + \mathrm{j}\ 10^{mlog(\frac{\omega_{max}}{\omega_{min}})} \tag{4.6}$$

Considering the previous frequency range the Eq. 4.6 can be written as follows:

$$p(m) = \sigma + \mathrm{j}\ 10^{\frac{m}{400}-2} \tag{4.7}$$

Eq. 4.5 can be used to analyze step or semi-infinite signals, such as a pulse or exponential decaying series. Moreover, it is possible to simulate open and feedback loops of a system mathematically, and margin finds gains for the stability of the system. Eq. 4.5 is used in the next section to analyze the stability of a boost converter current control of the proposed topology that is found in third chapter.

4.5 Buck-Boost converter current control using Inverse Laplace Transform

The proposed topology in chapter three has a DC-DC converter that can behave as a boost, buck or buck boost converter. This is because the effect of DC-link voltage modulation. The current control of the DC-DC converter in this chapter focuses more on the boost converter stability analyses for a couples reasons. Firstly, the stability of a boost converter request more parameters compared to a buck converter. Henceforth, the stability of a boost converter can guaranty the stability of a buck converter. Secondly, a boost and a buck-boost converter have analogous model [16]. Therefore, the transfer function modeling of the DC-link converter of the topology (Fig. 3.1) is based on a buck-boost converter. Fig. 4.3 presents equivalent circuit of buck-boost converter from the figure 3.1. This simple definition of the Inverse Laplace Transform has been used to analyze the stability of the proposed topology.

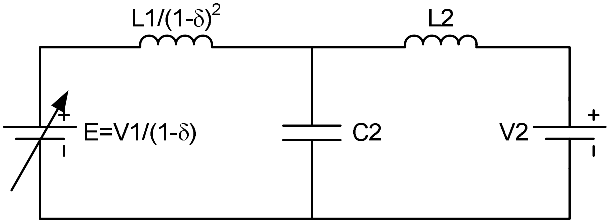


Figure 4.3: Equivalent circuit of buck boost converter

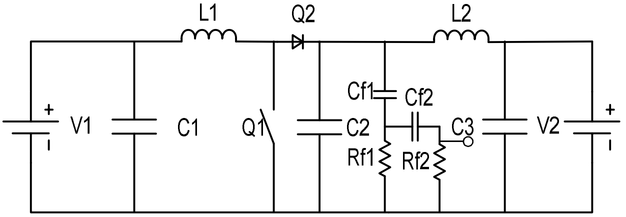


Figure 4.4: Buck-boost converter with high pass filter

The circuit is drawn after considering the continuous conduction mode [CCM] and its small signal deviations. V_2 is the voltage at the level of inverter. To stabilize the LC filter and to compensate its response delay, the high pass filter is integrated in the topology. Fig 4.4 shows the boost converter current control with the high pass filter.

Considering Eq. 4.7, the high pass filter transfer function can be expressed by Eq. 4.8. The single order high pass filters did not give enough phase advance.

$$H_{hp}(s) = \frac{1}{1+\frac{1}{\lambda_1 p}} \frac{1}{1+\frac{1}{\lambda_2 p}} \mathrm{e}^{-Td_1} \tag{4.8}$$

Where, $Td1$ is a delay for digital sampling, ƛ1 and ƛ2 are time constant for the high pass filter 1 and 2 respectively.

Table 4.1: Buck-Boost components

Components	Types of Components	Values
Capacitor, C1	Electrolytic	3*2200 μF
Capacitor, C2	Polypropylene film	20 μF
Capacitor, C3	Polypropylene film	10 μF
Inductor, L1	Amorphous iron	700 μH
Inductor, L2	Amorphous iron	1400 μH
Resistor,Rf1	Through Hole Resistor Axial Carbon Film	5kΩ
Resistor,Rf2	Through Hole Resistor Axial Carbon Film	50kΩ
Capacitor, Cf1	Film	10nF
Capacitor, Cf2	Film	1nF

The values of the second high pass filter are Rf1=5 kΩ; Rf2=50 kΩ; Cf1=10 μF, Cf2= 1μF (Table 4.1). Using the high pass filters then ג1=5*10^{-5} and ג2=1*10^{-4}.

Considering Fig. 4.3, the dynamic behavior of the topology and its CCM case, the transfer function can approximately be formulated by Eq. 4.9.

$$H(p,\delta) = \frac{RL2 + p\,L2}{\frac{(RL1 + p\,L1)\,[p\,C2\,(RL2 + p\,L2)]}{(1-\delta)^2} + RL2 + p\,L2} \tag{4.9}$$

Where *R, L1, L2, δ* are parameters of the topologies.

The open loop system transfer function in Eq. 4.10 is a product of Eq. 4.9 and Eq. 4.8.

$$HTF = H_{(hp)}\,H(p,\delta) \tag{4.10}$$

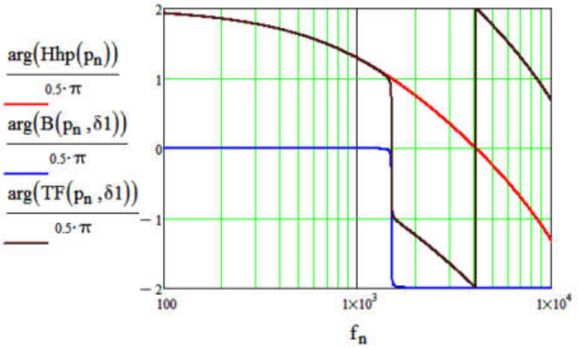


Figure 4.5: *TF1* open loop phase versus frequency

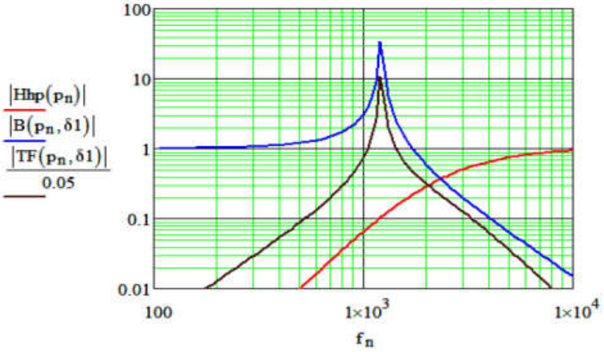


Figure 4.6: *TF2* open loop magnitude versus frequency

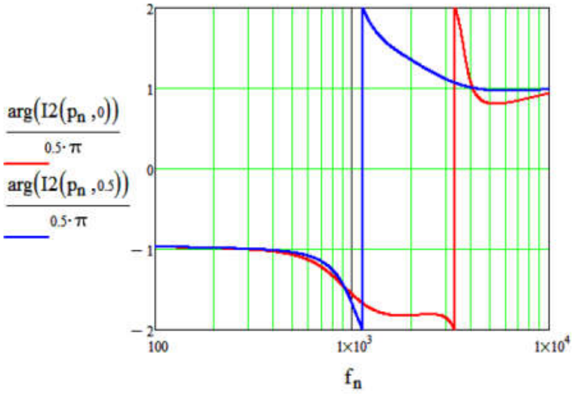


Figure 4.7: *I2(p,δ1)* closed loop phase versus frequency

The bode diagrams of the open loops of the high pass filter in Fig. 4.3 and Fig. 4.4 can help to figure out the current feedback loop transfer function. In fact, Fig. 4.5, Fig. 4.6 and Fig. 4.7 give the stability limit information of the system. Around the gain of 12 the system oscillates. Therefore, the gain margin less than 12 can make the system stable. The chosen gain is 5 for the current feedback loop. The transfer function of the current feedback is found in Eq. 4.11.

$$I2(p,\delta) = \frac{B(p,\delta)}{1 + B(p,\delta)\, H_{hp}(p)\, G_{hp}} \frac{1}{RL2 + p\, L2} \tag{4.11}$$

Where G_{hp} is the gain of the high pass filter.

The dynamic behavior in Fig. 4.8 and Fig. 4.9 is found based on the Eq. 4.11. Since the feedback is a PI type, Fig. 4.7 and Fig. 4.8 present the limit of the resonant frequency, which are useful to tune the PI parameters. Based on them, the PI transfer function is calculated [Eq. 4.12].

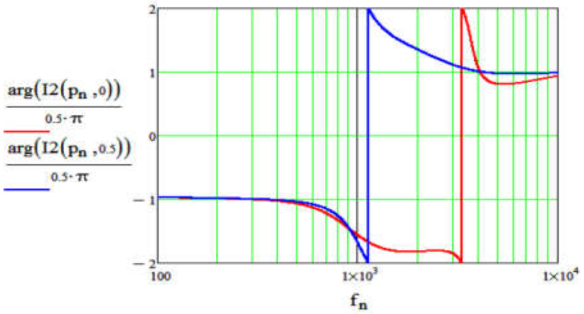


Figure 4.8: *I2(p,δ1)* closed loop phase versus frequency

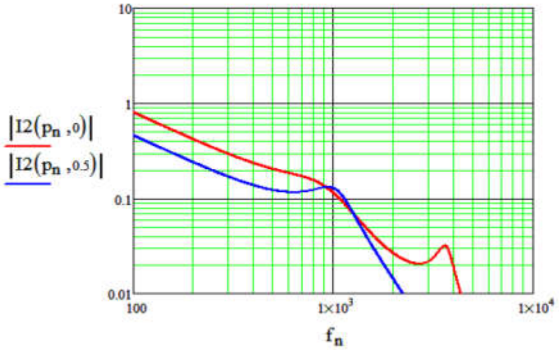


Figure 4.9: *I2(p,δ1)* closed loop magnitude versus frequency

$$PI(p,\delta) = \left[\frac{3000\,(1-\delta)}{p} + 4\right] \mathrm{e}^{-p\,Td2} \tag{4.12}$$

Where *Td2* is the delay of the PI controller.

The Open Loop Transfer Function (OLG) of the current in the second inductor combined with the transfer function of the PI controller is in Eq. 4.13.

$$OLG(p,\delta 1) = I2(p,\delta)\,PI(p,\delta) \tag{4.13}$$

For the tuned parameters, the system is stable. The pole is at one in left side.

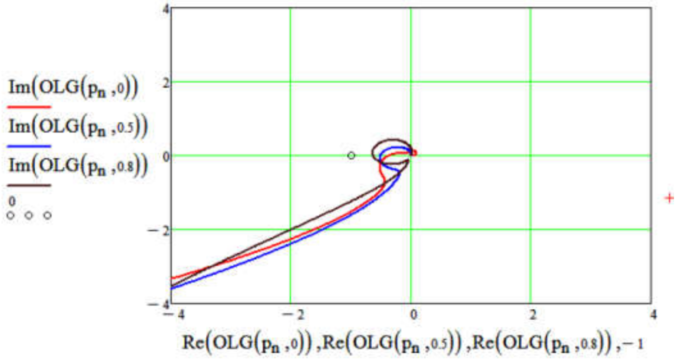


Figure 4.10: OLG Imaginary versus Real part Nyquist

Fig. 4.10 shows that for different values of delta, 0.0, 0.5, 0.8, the system is stable. The total feedback transfer function of the system can be calculated by Eq. 4.14.

$$TFI(p,\delta) = \frac{1}{1 + \frac{1}{OLG(p,\delta)}} \qquad (4.14)$$

Applying Eq. 4.4 and Eq. 4.5 on Eq. 4.14, the following equations can be formulated. The equations can lead to Eq. 4.15.

$$f(t,\delta) = \frac{2}{2\pi}\int_{\omega\text{min}}^{\omega\text{max}} \left[\frac{\mathrm{e}^{(\sigma+\mathrm{j}\,\omega)t}}{\sigma+\mathrm{j}\,\omega}\,(TFI(\sigma+\mathrm{j}\omega,\delta))\right]\mathrm{d}\omega \qquad (4.15)$$

$$f(t,\delta) = \frac{2}{2\pi\mathrm{j}}\sum_{m=0}^{n}\left[\big(p(m+0.5) - p(m-0.5)\big)\frac{e^{P(m)t}}{p(m)}\,(TFI(m),\delta)\right] \qquad (4.16)$$

The step response of the transfer function can be test by using Eq. 4.17 as input signal, where a slow square wave is used instead of a step wave.

$$f(t) = \sum_{\mathrm{k}=0}^{100} \frac{\frac{2}{\pi}}{2k+1} \sin[(2k+1)\omega\, t] \tag{4.17}$$

Where *k* is a real number, *k* ϵ R

The step response can as well be applied, but at least, 100 harmonics are needed at least to lower the Gibbs effects [17]. It is slow if a low frequency step wave is applied. It is, moreover, difficult to check if an overshoot is present or not. It can be formulated using a complex Fourier Transform [Eq. 2.18].

$$f(t) = \sum_{\mathrm{k}=0}^{100} \frac{\frac{2}{\pi}}{2k+1} \, \mathrm{Im}[\mathrm{TFI}[(2k + 1)\, \mathrm{j}\omega\, t\, \delta]\, \mathrm{e}^{(2k+1)\mathrm{j}\, \omega\, t} \tag{4.18}$$

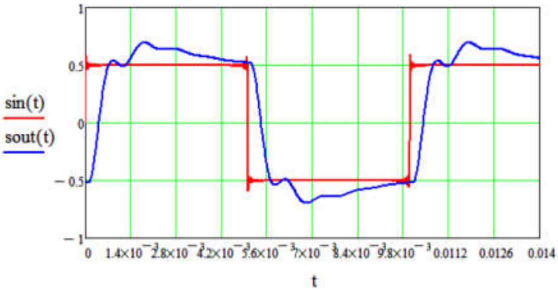


Figure 4.11: Step response at $\delta = 0.5$

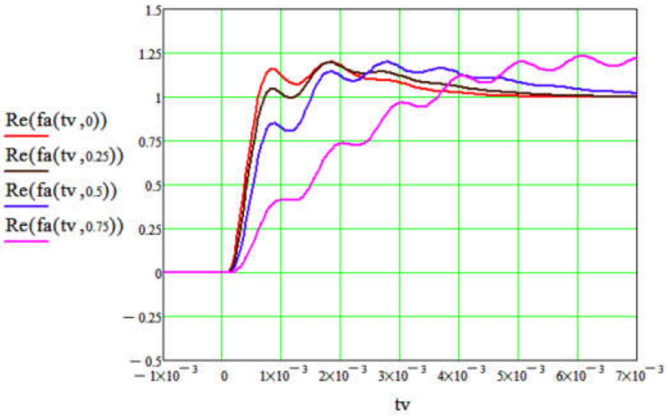
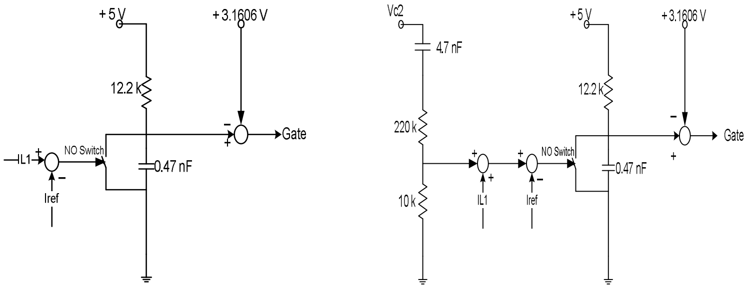


Figure 4.12: Step response of Eq. 4.15 and Eq. 4.16

Fig. 4.11 and Fig. 4.12 result from Eq. 4.18. It is obvious that the step response has periodically the Gibbs effects. It can be reduced by varying the duty ratio. At duty ratio which is equal to 0.5 the Gibbs effect reduces.

4.6 Buck-Boost converter current control Matlab Simulation

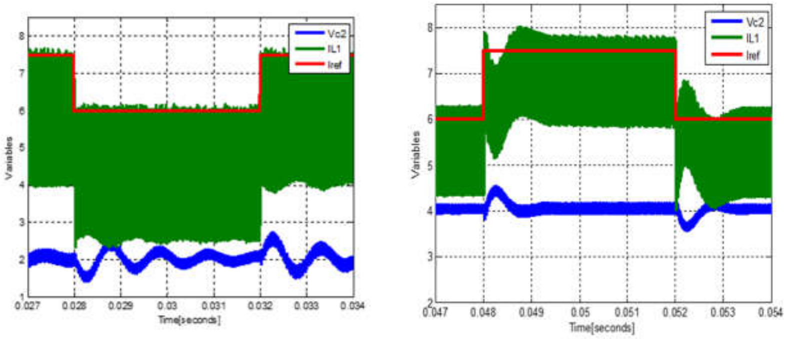
In order to confirm the accuracy of the step response test using the Inverse Laplace Transform control, the same test was carried out using Mathlab/Simulink. The tuned parameters used to test the boost converter. The test conducted for two current control techniques: The constant off time peak current control (COPCC), and PWM High pass filter feedback control. The two techniques were discussed deeply in the published paper that is in a connection with the present work [5]. The constant off time peak current control (COPCC) would have the advantage that it includes the protection in the control [5][18].The drawback of the COPCC is that it is not easily implemented in DSP technology.



(a) (b)

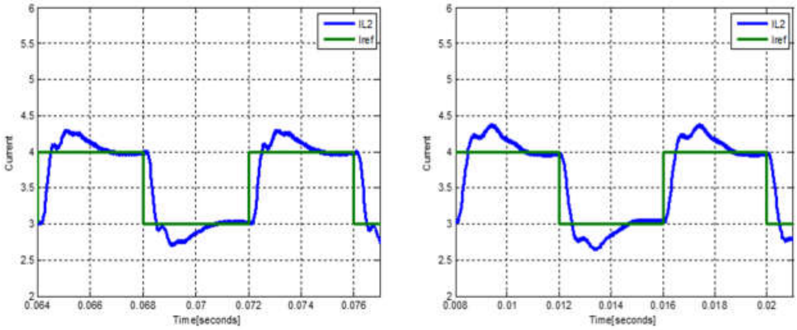
Figure 4.13: Constant off Time Peak Current Control Circuit: (a) without high pass filter feedback; (b) with high pass filter feedback

The advantage is that it will need only a single order high pass filter feedback to improve stability. The present chapter presents the Matlab simulation and related lab experiment of a PWM control. The PWM control needs a second order high pass filter feedback for improving the phase margin close to the resonance of the DC-link film capacitor and the inductors. In fact, the current in L2 cannot be controlled directly while switching the left leg of the proposed topology in chapter three. The present work focuses only on the Matlab simulation of PWM high pass filter feedback control. Fig 4.13 shows a COPCC: (a) without high pass filter feedback; (b) with high pass filter feedback. Fig 4.14 shows Matlab simulation result of the COPCC. Fig 4.14 (a) shows that there is some resonant frequency once HPF is not used. It is clear on (Fig 4.14 (b)) that COPCC with HPF feedback stabilizes the system. The system is being damped and has a reasonably fast step response.



a) b)

Figure 4.14: Constant off Time Peak Current Control Circuit Matlab simulation: a) without high pass filter feedback; b) with high pass filter feedback



a) b)

Figure 4.15: I_{ref} and IL2 while controlling the Boost converter (a), I_{ref} and IL2 while controlling the Step down converter (b)

To put an electrolytic capacitor at the output simulates a low impedance V2, the grid impedance in the simulation. The PWM with HPF was employed to test the stability of the DC-DC part. Some concerns of digital control drawback have been considered. The main drawback of digital constant frequency control is that one introduces a delay due to sampling, conversion to digital, calculating and applying it to compare with a saw tooth If done well there is typically about one period delay in the control of a duty ratio. A low pass LCL circuit has typically almost no phase shift at low frequency and 180° phase lag at high frequency. So, to damp the resonance, a 90° phase lead should be given. Moreover, some phase advance to compensate for the delay of the processor based PWM. To obtain that it seems that a second order high pass filter performs much better than a first order. This has been implemented in Matlab simulation. Fig 4.13 shows that the buck and the boost current dynamic response is fast.

4.7 Buck-Boost converter current control lab experiment

The step up is mainly composed of the power stage (top side), the constant off time current control (middle part), and the over voltage protection (bottom part) [Fig. 4.16].

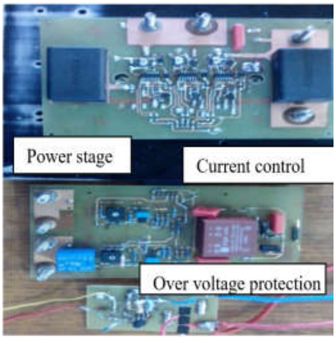
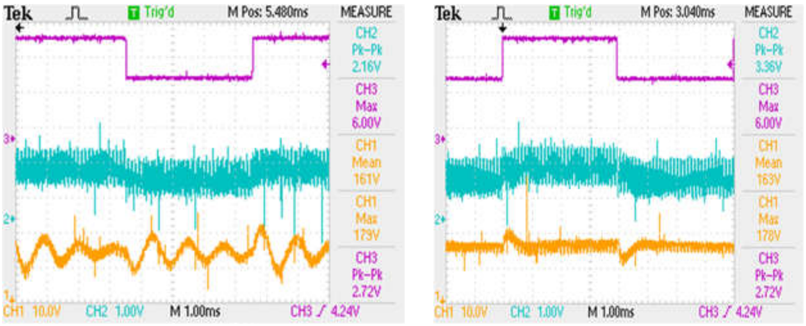


Figure 4.16: Buck-Boost converter step Up



a) b)

Figure 4.17: Constant off Time Peak Current Control Circuit lab experiment: (a) without high pass filter feedback; (b) with high pass filter feedback

The conducted experience is based on the simulation presented in the previous section. In the step up mode, the system is stable without feedback, whereas in the step down mode, the system is even unstable in open loop. The analyses of the system are made by referring on the simulation and lab experiments results. In [Fig. 4.17 a] and [Fig. 4.17 b], the channel 2 is the current, the purple channel is reference current and yellow channel is the voltage. The lab results and the simulation show a similar dynamics of the system. Fig. 4.17 show that the output voltage is 178 Volts. This is due to the fact that the input voltage was 89 Volts.

4.8 Conclusions

The proposed PV inverter topology will be subject to the disturbance from the grid and should be enough damped. The small capacitor at the DC-link is necessary for enough bandwidth but can impair the stability. Therefore, a tool of testing the stability of the DC-DC part has been employed. The test of the DC-DC part stability of the proposed topology has been conducted using mainly Numerical Inverse Laplace Transform. The results of this technique have been helpful to tune the control parameters of a PV buck boost converter. COPPC and PWM with HPF have been used to proof check the stability of DC-DC link of the proposed topology, the conclusion is that a feedback of the DC-link voltage improves the damping to a sufficient level. The next analysis can be extend to the H-bridge part of the topology. The chapter five focuses more on this concern.

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Chapter 5

Frequency synchronization using a Double Integration Method

5.1 Introduction

The fourth chapter investigated an instantaneous working point from the DC input to a specific momentary voltage in the AC grid. Yet, the DC-DC part of the topology must follow the reference current to be injected in the AC grid. Therefore, it must be synchronised according to the AC voltage. Typically a Phase Locked Loop (PLL) algorithm is used for that. The present chapter proposes an alternative technique. The technique is "Double Integration Method" (DIM) of frequency synchronization for a grid-connected inverter.

5.2 Phase Locked Loop drawbacks

First, it has to be noted that an obvious simple method is not suitable. "Voltage proportional to current control" is perfect for loads and it is used for power factor boost controllers. If this principle is used in generation, it creates an impedance with a negative real part also for frequencies different from the grid frequency [1]. This results in oscillations when high resonant frequencies occur in the grid. Also when paralleling inverters, it may create instabilities. Hence, the better way is to create a set value for a sine wave that is synchronized to the grid voltage but not proportional to the grid voltage.

A number of the grid connected PV inverter has been increased not only in developed countries but also in the developing countries. To obtain synchronization between the grid voltage and the inverter output current has been an issue that many scholars have published various research on it. Phased Locked Loop (PLL) control is most popular techniques that has been used for grid connected PV inverters [2],[3]. The author in [4] presented an overview of different PLL schemes (Table 5.1). Table 5.1 shows different PLL techniques and their performances. In general, Phase locked loop controller (PLL) techniques recognize the fundamental without making a 'negative resistor', but there is still a hidden dynamic phenomenon as well [5],[6]. Making a rotating vector or a known angle in the period requires a minimum of two independent phases in a system .

Table 5.1: List of some works on PLL

Related Work Reference	Type of PLL	The Simplicity of Design	Adaptive of Frequency	Distortion for Insensitivity	Balance Sensitivity
Masoud Karimi-Ghartemani and M. Reza Iravani [7], 2004	**EPLL**	★★	★★	★★★	★★★
Houshang Karimi et al [8], 2004	**QPLL**	★★	★★	★★★	---
Shinji Shinnaka [9], 2008	**RPLL**	★★	★★	★★★	---
Kyoung-Jun Lee et al [10], 2014	**APLL**	★★	★★	★★★	★★★
H. Shokrollah Timorabadi and F. P. Dawson [11], 2007	**PPLL**	★★	★★★	★★★	★★★
Sidelmo M. Silva [12]**, 2004**	**SFPLL**	★★★	★★	★★	★

Where **: ★★★ Good, ★★ Average and ★ Poor**

EPLL	Enhanced Phase Locked Loop;	**APLL**	Adaptive Phase Locked Loop
QPLL	Quadrature Phase Locked Loop;	**PPLL**	Predictive Phase Locked Loop
RPLL	Robust Single Phase Locked Loop;	**SF-PLL**	Synchronous Frame Phase Locked Loop

The single-phase inverter voltage output has only one phase and a second signal that would be needed in order to construct a second phase of 90° shift [13]. The more common used method is the phase locked loop control; however, it has a number of drawbacks. It does not use a second signal but it does use a phase comparator that has the tendency to inject a second harmonic in the feedback, which has to be filtered out by some kind of a notch filter [6]. The filtering can introduce an unwanted transient response [14]. Moreover, a system having a filtering subsystem increases computing time. The filtering system might be averaged over a half or full period. In addition, this needs time and it has a dynamic phenomenon that makes it difficult to start in the first periods when the grid is just enabled [15][16]. It is also difficult to model as it depends on software decisions when the loop gain is high to synchronize fast and a lower gain to be less sensitive to disturbances. To avoid the drawbacks of the briefly discussed methods, a double integration synchronization method (DISM) presented in this chapter can be used to synchronize the DC/AC current with the grid frequency. A pragmatic solution in practice could be to implement both and choose the best depending on the needs or application.

5.3 DISM for a Single Phase Inverter

The DISM is known technique. It has been used in different applications, however, the problem of the DC offset phenomenon has been its drawback [17], [18].The art of the method presented in this work is how to employ DISM and remove the integrating constants without degrading the signal in order to synchronize the frequency of the grid voltage with the inverter current.

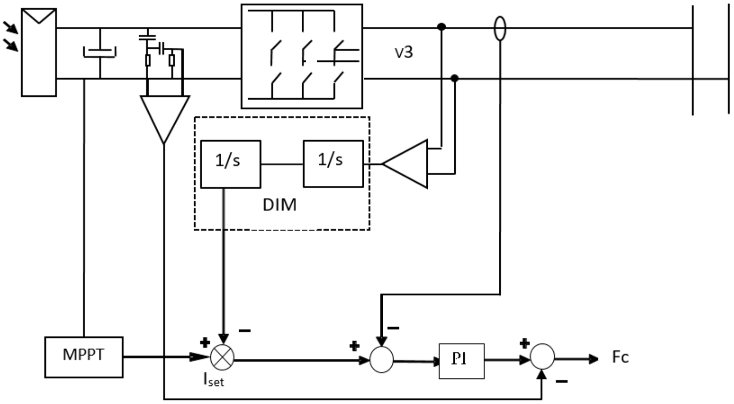


Figure 5.1: DISM scheme embedded in total control (without removal of integrating constant)

Fig. 5.1 shows the simplified principle of DISM. The double integration is applied on grid voltage, which is multiplied with the set current. For the PV case, the set current is from a MPPT (Maximum Power Point Tracker). The set current is compared to measured current. The PI control is applied to generate a duty ratio to correct the current error. Based on the DISM response, the PWMs are generated and they control the H-bridge inverter and the buck boost converters.The DISM uses the grid voltage as an input. Considering some perturbations, Eq. 5.1 presents the voltage after disturbance.

$$V(t) = A_1 \sin(\omega_1 t) + \sum_{n=1,3,5,7} \frac{2V_{\mathrm{DC}}}{\mathrm{n}\,\pi}[B_n \cos(\omega_n t)] \qquad (5.1)$$

Where V_{DC} is the DC-link voltage, $\omega_1 t$ and $\omega_n t$ are angular rates for fundamental and disturbances signals. A_1 and B_n are amplitudes for a voltage signal and its disturbance respectively. The reference current can be obtained by integrating twice Eq. 5.1. The reference current will have a phase shift of -180°. It is obvious that the amplitude of the current is inverse proportional to the grid frequency. However, the current phase synchronizes with the voltage phase. To make the control system presented in the Fig. 5.1 more effective, the DC offset of the integrator has to be removed. However, removing the offset by the feedback should not interfere with forward integrator in a continuous mode, as it might introduce a phase shift or harmonics. The modeling of DSIM using analogue equivalent circuit makes the concept easily understandable.

5.4 Analog equivalent for removing offset

The application of the above DSIM principle has normally been limited by the presence of an integrating constant. The removal of the integrating constant has been a concern. Once the elimination of the integration constant is fast, it affects the phase accuracy of the double integrator. If it is slow, the control results in a long transient at start-up or after heavy disturbances, such as a large dip or a phase angle shift in the grid. A compromise leads to an understandable analog PI controller with a non-linear feedback. Fig. 5.2. shows the art of removing the integrating constant using an analogue circuit. The first operational amplifier integrates the grid voltage without considering the initial conditions. Since the non-consideration of the initial condition of a small offset can cause an integrating constant and/or drift in the output signal, the feedback integrator correct the offset based on the voltage across D1 and D2. The second integrating part is similar to the first part. R4, R2 and R3 are gains for forward and feedback integrators. The integrator has input signal *V(t)* is a state of derivative of its output signal *I(t)*. This can be more explained by Eq. 5.2.

$$I(t) = \int_{\mathrm{to}}^{\mathrm{t}} u(t)\,\mathrm{d}t + V_{20} \qquad (5.2)$$

Where, the input *u(t)* and *I(t)* are input and out signals respectively.V_{2o} is the initial condition.

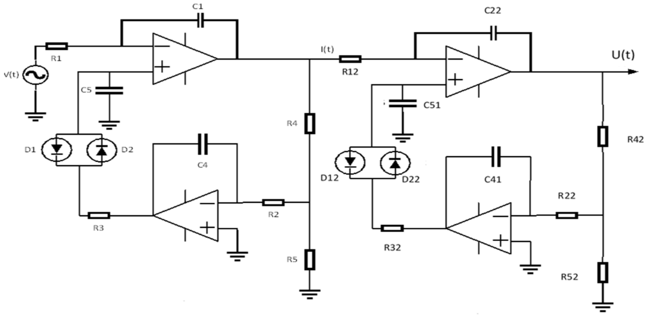
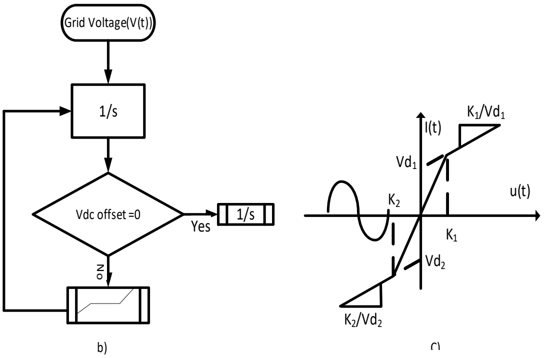


Figure 5.2: DISM with removal of integrating constant analog concept



a) b)

Figure 5.3: DISM with removal of integrating constant concept algorithm, Vd2=-Vd1,K1=-K2

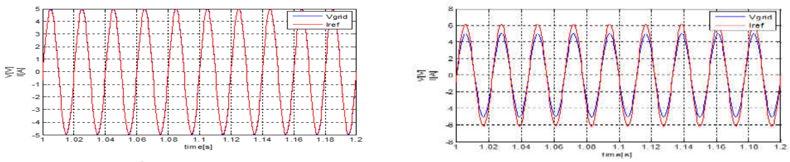
Fig. 5.3 a) and Fig. 5.3 b) explain more the concept presented in Fig. 5.2. Both figure show the dead zone control. This dead zone control is implemented using diodes (Fig. 5.2). Eq. 5.3 is formulated based on Fig. 5.3 b) and on Eq. 5.2.

$$I(t) := \begin{cases} \dfrac{K_1 u(t)}{\mathrm{V_{d1}}} + K_1 & \text{if } I(t) \geq V_{\mathrm{d1}} \\ \dfrac{K_1 u(t)}{\mathrm{V_{d1}}} - K_1 & \text{if } I(t) \leq -V_{\mathrm{d1}} \\ \left(\dfrac{K_1 + \frac{V_{\mathrm{d1}}}{K_1}}{V_{\mathrm{d1}}} \right) u(t) & \text{if } -V_{\mathrm{d1}} \leq I(t) \leq V_{\mathrm{d1}} \end{cases} \qquad (5.3)$$

Where V_{d1}, V_{d2} are D_1 and D_2 voltage drop respectively. The voltage drop is estimated at 0.6 Vdc that are boundary conditions that are used to investigate if the input signal has high gain or low gain. K_1 and K_2 are coefficients of I(t). In order to control the drift, K_1 and K_2 are -1 and 1respectively. D1 and D2 are employed to define the break points of the boundaries. For the third and the fourth case, the drift phenomenon is avoided to happen. Whereas for the first and the second case, the integrator auto reset has to be handled by the feedback integrator. The interval between peak points is used to add or subtract a constant value to the input signal which is scaled by the slope of the dead zone interval. This is done for the first and the second Integral. Hence, Eq. 5.3 is a key tool to implement DISM digitally. The following paragraph explains the dynamics behavior of the DISM in Matlab and Simulink.

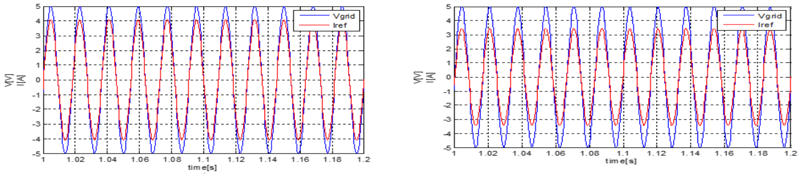
5.5 DISM Simulation

The DISM simulation was done in Matlab & Simulink. The forward and feedback integrator sampling time are f_s and $1/4*f_s$ respectively. Hence, the forward integrator is faster than the feedback integrator is. This helps the algorithm to detect and remove the drift phenomenon so that the integrator resetting can take few milliseconds. The Fig. 5.4(a), Fig. 5.4(b), Fig. 5.4(c) and Fig. 5.4(d) present the synchronization of an inverter current to the grid voltage frequency at 50 Hz, 45 Hz, 55 Hz and 60 Hz, respectively. At 50 Hz, the blue line is not clear because there is a perfect synchronization both in a phase and in the amplitude. The reference current is synchronized with the grid voltage. However, the variation of the frequency affects the reference current amplitude.



a) Synchronization at 50 Hz

b) Synchronization at 45 Hz



c) Synchronization at 55 Hz

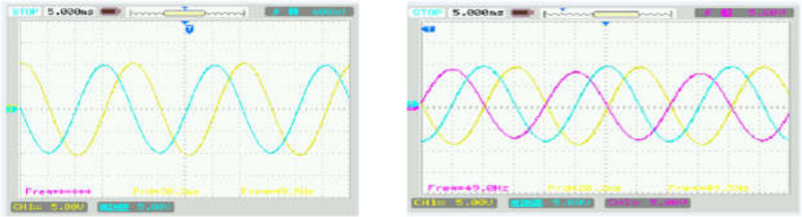
d) Synchronization at 60 Hz

Figure 5.4: DISM Matlab simulation

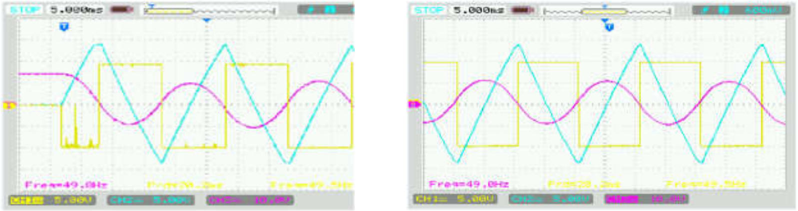
The higher the grid frequency becomes, the lower the current amplitude becomes. This can be corrected by the MPPT (Fig. 5.1) or a gain value in the control after some periods. On a short time transient, the grid frequency rises and a small amount of current is injected into the grid. For more power injected to the grid, the inverter frequency decreases. If the grid is connected to a PV panel converter, the MPPT will restore the frequency after some periods by adjusting the power grid [12]. The DISM rejects the amplitude of harmonics. A third harmonic is reduced by a factor of 9, a fifth is reduced by a factor of 25, which is enough in practice. If a square wave is applied, 1/27 third harmonic is expected compared to the fundamental and 1/125 for the fifth harmonics (Eq. 5.2). Consequently, the value of the reference current does not content significant harmonic component.

5.6 Lab experiments

Before implementing digitally the double integrator synchronization method for the entire system, the analog circuit has been tested to test the dynamics of the system. The analog system has been used to understand the fundamentals and calculate and tune well the gains of the first and the second integrator. A simple operational amplifier, TL084, was used to conduct the experiment. In the Fig. 5.5(a), the first integrator is in blue and it lags 90° to the original signal. In Fig. 5(b) the second integrator output in purple is synchronized with the input signal, grid voltage, in yellow after being amplified by a gain of k=-1.



a) Synchronization at 50 Hz b) Synchronization at 45 Hz



c) Synchronization at 55 Hz d) Synchronization at 60 Hz

Figure 5.5: DISM measurement on the analog circuit

In fact, the second integrator could be -180 ° phase shift referring to the input signal. The circuit is simple and works well for the grid (50x (1±10%) Hz and (60x (1±10%) Hz. Practically, it can handle frequencies from 40 to 70 Hz. Of course the output amplitude is lower in the case of 60 Hz. However, the amplitude of the set value for the current has anyhow to be adapted as it is also proportional to the output of the MPPT controller.In this way, a variable amplitude in the current set value to the grid is achieved. Making a variable gain is not so easy in analog, therefore, the digital system, modern technology, is much more practical, but the analog system was still rather easy to build and simulate, it fulfils the principle to compare two concurrent implementations to have some self-auditing. Fig. 5.5(c) presents the transient state of the input signal, square wave form, at a starting point and Fig. 5.5(d) presents the steady state of the input signal. The square wave form signal was used to test if the DISM does not deteriorate the input signal. Note that even with a square wave input, the output is close to sine wave, in fact it is a sequence of parabolas, for example the third harmonic is 1/27th of the fundamental. The DISM, a nonlinear feedback, is always active at different frequencies. Its optimal control can be reached in the smallest amount of time. Moreover, the grid voltage signal cannot be deteriorated.

5.7 Conclusions

A double integration synchronization method (DISM) is an alternative synchronization method for a DC/AC grid tied frequency. The chapter presents how the integrator initial constant can be removed in order of not deteriorating the input signal. It delivers useful signals from the first period. The DISM is simpler to program and to simulate than a PLL. Some simulations and lab experiments that can be applied on real system are presented in this chapter to show the dynamic performance of the DISM. It could be used to help a fast start of the grid after a shutdown.

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Chapter 6

Gate driver design

6.1 Introduction

From chapter three to chapter five, the book has been focusing on the performance of the power stage and control of the proposed topology. It has shown the effect of avoiding or reducing the use of an electrolytic capacitors. Often also electrolytic capacitors are hidden in gate drives or internal power supplies. Hence, a design of a gate driver must consider it. A ruggedized current protection, independent from software, is also desired for the gate driver. If possible a very low stand-by consumption must be achieved. Moreover, a low capacitance over the galvanic separation must considered as it influences the radio frequency EMI performance. The proposed gate driver gives an answer to such a problem setting.

6.2 Gate driver circuits drawback

To turn ON and OFF the IGBTs or MOSFETs, as well as other gate controlled power switches, a gate drive circuit is needed [1]. The gate driver circuit has by preference a galvanic insulation capability between the controlling signals and the power [1]. Many IGBT gate driver circuits with different methods have been proposed [2]. Some gate driver circuits have application limitations as they can fall in an unsafe mode for some cases and some others do have a complex design with two or more power supplies with different levels which can have a common power supply point [3]. A typical problem is what happens if the internal supply is lower than its rated value. It happens typically at shutting down or interrupted grid. A common power supply at the lower transistor side must also be avoided as it results in large circulating currents due to the parasitic source inductances. This is typically observed in the bootstrap gate driver circuits since they are not galvanic separated. To overcome these challenges, a snubber energy regeneration or charge pump technique is often used for the high-side gate driver of an inverter. However, during high current applications, these techniques are limited because they presents quite high power losses [4], [5].

Nevertheless, based on the switching behavior of an IGBT, all gate drive circuit designs must have common performance to force the converters operate in safe mode [6]. The authors in [7] and [8] have deeply explained the state-of-the-art related to the IGBT gate driver concepts.

The gate driver circuit design must consider the effect that the inverters drive the inductive loads which cause losses during switching period by the reverse recovery of the diode. A typical example can be observed based on IXFB82N60P power MOSFET, where the diode recovery charge at d*i*/d*t*= 200 A/µs. if a used gate driver circuit has a parasitic inductance of *L*=20 nH (about 20 mm of the length of a track), the system can easily have an inductive drop of 4 V. Ideally, a designer would like to have a completely independent gate driver with its own local supply. However, this is often considered as too expensive or having too much losses due to parasitic inductance and capacitance. The present design brings an idea of designing an IGBT gate driver circuit with a local supply for each transistor and low parasitic capacitance between the gate driver and the controller. The proposed gate driver has also a desaturation protection capability. Fig. 6.1 presents the gate driver circuit concept with an inductive 1:1 component of low cost (about 0.5 Euro/item) and low inductance, it seems that the component has a very low no-load loss although it is sold as a "common mode filter", but has a very large market due to that. A low cost inductive component is not only the feature of the gate driver but also one square wave supply that can be used to drive local supplies, six inductive components, is a key feature of the gate driver.

6.3 Features of the proposed IGBT gate drive circuit

The circuit in Fig 6.1 has three main parts. The first part is power supply. It consist of a transformer that can be supplied by a square wave power supply, a Schottky diode bridge and some capacitors. The second part is a galvanic signal isolation that consists of an opto-coupler-driver. The third one is desaturation protection. Each part is detailed in the following section. In order to be able to use a variety of gate drivers, the desaturation is done using the under voltage lockout of the driver, it has also the advantage to slow down the emergency turn-off to avoid a high peak voltage afterwards [9].

6.3.1 IGBT less-conventional gate drive supply

A power supply of a gate driver must not be easily disturbed by the return current injected by d*v*/d*t* which occurs during the switching off period of the power transistors but also it must be low loss [7],[10]. The published paper on this topic [11] found that "off the shelf", 'block DC-DC power supplies', have a considerable capacitance between the two sides which is in order of 47-220 pF. This creates a heavy inter-disturbance between a power supply and a gate driver. Fig. 6.1 shows the proposed IGBT gate driver. The first part presents the power supply. The power supply has the features of the Under Voltage Lock Out (UVLO) capability [12]. The used transformer, a common choke filter, has a galvanic insulation voltage rating of 4000 V DC and low stand by consumption of less than 8 mW per one leg at no-load.

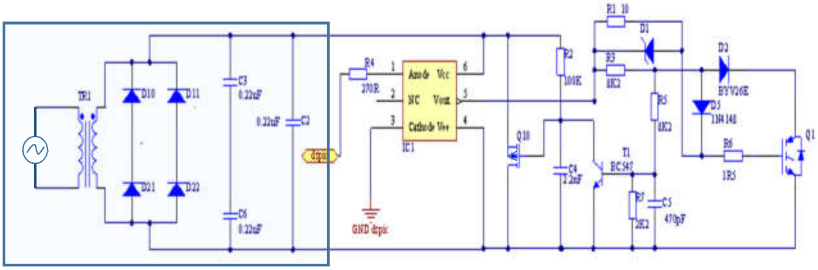


Figure 6.1: A Proposed IGBT gate drive

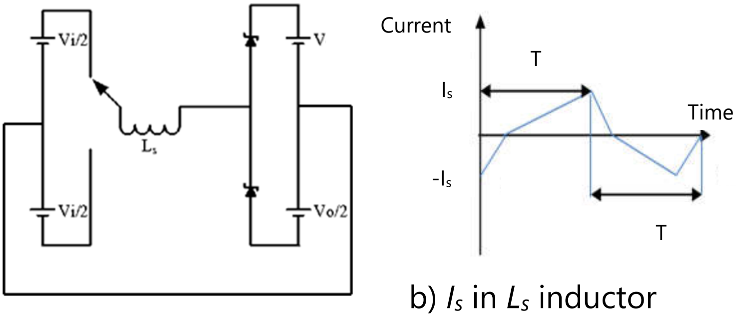
Table 6.1: Parameters of the KEMET 07010 common mode filter used in the gate driver

Parameters	**Values**
Magnetization inductance (measured)**	1.6 mH
Insulation primary secondary (rms, during 2s)**	2.4 kV
Primary secondary coupling capacitor**	3 pF
Primary turns**	43
Secondary turns**	43
Rated current AC*	0.7A
Maximum DC resistance(Line) *	0.6 Ω
Rise temperature *	40 K
Short circuit L-R impedance at 1KHZ**	32 µH, 1.017 Ω
Short circuit L-R impedance at 100 kHz**	31.16 µH,0.86 Ω
Apparent Permeability**	2753
Magnetization losses at 7.5V peak square**	8.23 mW
Al value = permeance Λm**	865nH/turn^2
**Measured parameters * Data from data sheet	

The specification parameters of the transformer are found in Table 6.1. The transformer has the parasitic capacitance of 2 pF. The reason of this low capacitance takes origin from windings in separate rooms. The leakage allows the gate driver to shut down easily using the supply pulling it into under-voltage lock-out mode. In this topology, a design without electrolytic capacitors was achieved in order to increase lifetime of the gate drive. Fig. 6.2 presents an equivalent electrical circuit of the power supply which compasses a half-bridge rectifier circuit and an inductor of a common choke filter used as a transformer. In the figure, the output voltage has a lower voltage than the input to analyze the load performance of the transformer. So, Eq. 6.1 can be derived from the figure and be employed to evaluate the current.

$$\frac{\mathrm{d}i}{\mathrm{d}t} = \frac{V_\mathrm{i} - V_0}{2L_s} \tag{6.1}$$

Eq. 6.1 expresses the current variation in the positive slope. Fig. 6.2 and Eq. 6.1 explains the current variation in negative slope. Where , V_i, V_o, I_s, I_out ,f and L_s are input voltage, output voltage, inductor current, output current, frequency and series inductor, respectively.



b) I_s in L_s inductor

a) Half-bridge circuit

Figure 6.2: Half-bridge circuit and I_s in L_s inductor

$$\frac{\mathrm{d}i}{\mathrm{d}t} = \frac{V_\mathrm{i} + V_0}{2L_s} \tag{6.2}$$

Combining the Eq. 6.1 and Eq. 6.2, Eq. 6.3 is formulated.

$$\frac{T}{2} = \frac{2L_s + I_s}{V_\mathrm{i} - V_0} + \frac{2L_s + I_\mathrm{s}}{V_i + V_0} \tag{6.3}$$

Solving Eq. 6.3 for $I_{s,}$ It gives Eq. 6.4.

$$I_\mathrm{s} = \frac{T \times L_s \times V_\mathrm{i}}{8 \times \left(V_\mathrm{i}^2 - V_0^2\right)} \tag{6.4}$$

Hence, the DC output current is calculated as follows:

$$I_\mathrm{out} = \frac{T \times \left(V_\mathrm{i}^2 - V_0^2\right)}{32 L_s V_i^2} \tag{6.5}$$

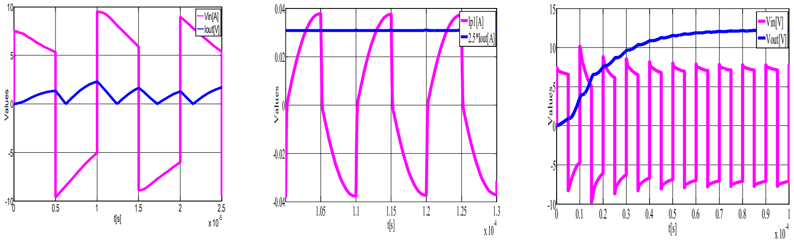
Since the impedance is contains also a capacitor, and the main current is caused by the fundamental, the rectified short cicuit current, I_{out} can be approximated by using by Eq. 6.6.

$$I_\mathrm{out} = \frac{2V_\mathrm{i}}{\pi^2 Z_\mathrm{LC}} \tag{6.6}$$

It is clear that a limited value of the capacitor increases the short circuit current for a given frequency. But, as a limited short circuit current is prefered, the series capacitance should be higher than the one that would resonate with the leakage inductance. Eq. 6.7 can be found by considering the Eq. 6.5 and Eq. 6.6.

$$I_\mathrm{out} \approx \frac{T \times \left(V_\mathrm{i}^2 - V_0^2\right)}{32 L_s V_\mathrm{i}^2} \left| \frac{\mathrm{j}2\pi L_s}{R_r + \mathrm{j}2\pi f L_s + \frac{1}{\mathrm{j}2\pi f C_s}} \right| \tag{6.7}$$

Where f = 100 kHz. The R_r is approximately 3 Ω. The main voltage drop is due to the leakage inductance.



a) b) c)

Figure 6.3: Transformer input, V_{in} and output voltage, V_{out} (a) I_{out} at R_{load} =0.1 Ω ; (b) R_{load} =1 kΩ , (c) R_{load} =10 kΩ

In fact, The R_r does not influence much the result. Eq. 6.7 can be used to analyze the power consumption of the gate power supply with different load resistance. The power supply voltage can be pulled down when the current remains still at an acceptable value, even when the load is close to the short circuit. The consumed no-load power is 3.3 mW/drive. When the load becomes 10 kΩ, the output voltage is 13.2 V DC as shown in Fig. 6.3. Fig. 6.3 shows the power supply when R_{load} becomes close to the short-circuit.

6.3.2 Opto-coupler

Many gate driver circuits use an opto-coupler technique to switch ON and OFF the IGBTs. The opto-couplers have same features with different values. It is upon a designer to choose the adequate parameters that are related to his application. However, some major factors like the gate resistor value, the power and the current to be delivered to the IGBT must be considered. Fig. 6.1 optimally uses the ACPL-P341 opto-coupler.

Table 6.2 ACPL-P341 Properties

Parameters	Values
Insulation	6000 V (peak)
Output current	3 A (peak)
Max. Supply Voltage	30 V DC
Input voltage	1.2-1.9 V DC at Infract Red diode
Input current	10 mA at Infract Red diode
Input-output capacitor	2 pF
UVLU ON	Max. 13.5 V DC
UVLU OFF	Min. 11.1 V DC
Power dissipation	Max.700 mW
CMTI	>35 V/ns
UVLU Under Voltage Lock Out, CMTI = Common Mode Transient Immunity.	

Table 6.2 shows the characteristics of the used opto-coupler. The supply current is less than 3 mA which means 45 mW at 15V. The parasitic capacitance between LED and screen is 2 pF. Considering the parasitic capacitance of the gate power supply, 2 pf, the total parasitic capacitance becomes 4 pF. To avoid a too high dv/dt at turn on and a spurious turn on in the off state, the opto- coupler drives the IGBT gate trough *R1*= 10 Ohms and *R6*= 2 Ohms.

6.3.3 Desaturation Protection Circuit

IGBT desaturation protection circuits have been used since the beginning of the IGBT and even bipolar technology. However, the technology has been getting upgraded in between. With the actual technology, the transconductance (gm) has been increased. And the magnitude of the IGBT short-circuit is directly proportional to gm [12]. For this reason, during a short-circuit period, a higher collector current can occur [12]. In this case, a very fast desaturation protection is needed. A two steps method can be employed [8]. This protection technique is mostly appropriate for the turn off the IGBT [8]. The desaturation protection in Fig. 6.1 monitors the IGBT threshold voltage and at low impedance it pulls down the gate drive supply voltage using MOSFET Q10. Consequently, the power supply of the driver turns off by undervoltage protection. The low impedance during the off state avoids the d*i*/d*t* and the dv/d*t* that can cause the unexpected shoot trough current [13],[14]. The equations (6.9,6.10,16.11) explain clearly that the voltage at D5 and R6 is linked with dv/dt. More details are given in [15]. All parameters that can influence the fast variation of dv/dt must be very well controlled.

$$C_{\mathrm{GC}}\frac{\mathrm{d}V_{\mathrm{CE}}}{\mathrm{d}t}-C_{\mathrm{GC}}\frac{\mathrm{d}V_{\mathrm{GE}}}{\mathrm{d}t}-C_{\mathrm{GE}}\frac{\mathrm{d}V_{\mathrm{GE}}}{\mathrm{d}t}-i_{\mathrm{G}}=0 \tag{6.9}$$

$$V_{\mathrm{GE}}-i_{\mathrm{G}}\mathrm{R}_{\mathrm{G}}-\mathrm{L}_{\mathrm{S}}\frac{\mathrm{d}i_{\mathrm{G}}}{\mathrm{d}t}-i_{\mathrm{G}}\mathrm{R}_{\mathrm{Ds(on)}}=0 \tag{6.10}$$

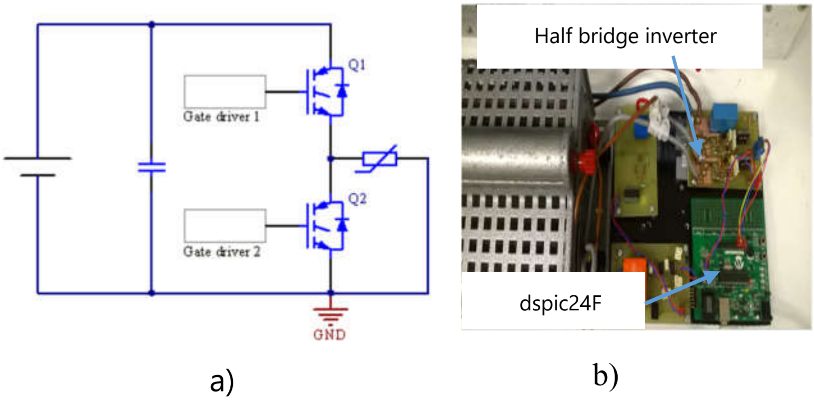
Where R_G is the gate resistance, L_s presents the PCB tracks and die bonding wires conductance, $R_{\mathrm{DS(on)}}$ represents the opto- coupler driver inductance. C_{GC}, C_{GE} and C_{CE} are respectively the gate-collector, gate- emitter and collector-emitter capacitances. Whereas, V_{GC}, V_{GE} and V_{CE} are respective voltages.

$$\frac{V_{\mathrm{GE}}}{V_{\mathrm{CE}}} = \frac{\mathrm{s}\left(R_G + R_{\mathrm{DS(on)}}\right)C_{\mathrm{GC}}}{1 - \exp\left(-\frac{R_G + R_{\mathrm{DS(on)}}}{L_s}\right) + \mathrm{s}\frac{\left(R_G + R_{\mathrm{DS(on)}}\right)}{\left(C_{\mathrm{GC}} + C_{\mathrm{GE}}\right)^{-1}}} \tag{6.11}$$

Eq. 6.11 shows that the pull down gate resistor must be small value to avoid that the gate emitter voltage increases. Moreover, it shows that the design of a PCB must consider Ls in order to prevent the self-turn ON of the IGBT.

6.4 Experimental set up

The paper presents the setup employed to test the gate drive circuit. Fig. 6.4 presents the Half bridge that is being driven by the gate driver, the dspic33FJ16GS402 used to generate the PWM set for the inverter, the current measurement, the DC power supply, low voltage power supply and the variable resistor as a load (0-10Ω). The half H-bridge has a mid-point that connect DC bus and ground. This can be a source of noise at any frequency value.



a) b)

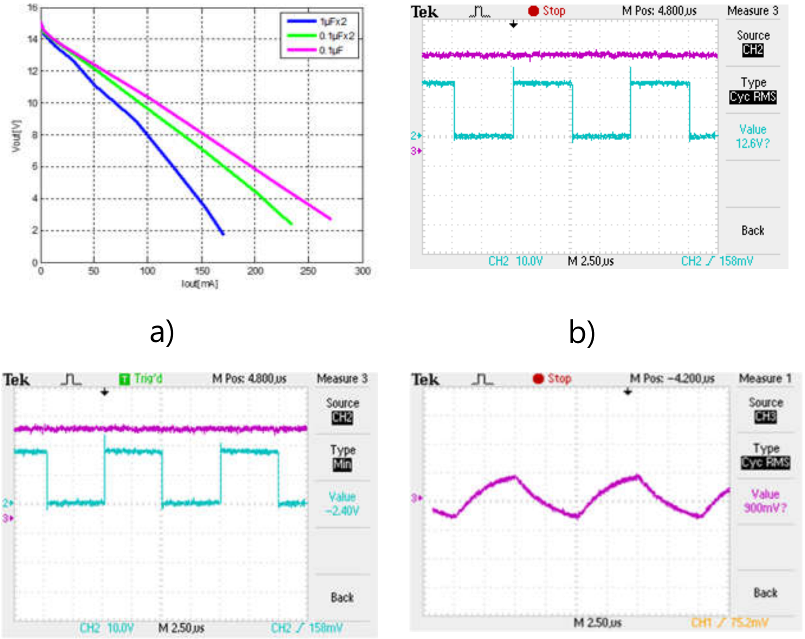
Figure 6.4: Experiment: a) gate driver testing circuit; b) Experimental set up

For this reason, the circuit is a good tool to evaluate if the designed gate driver with a low parasitic capacitance does avoid noise, which can take origin from the interference between low and high voltage signals. In other words, the circuit can be used to evaluate if there is not internal and external electrical magnetic interference (EMI). The circuit has three major parts. The gate driver, a half bridge inverter and a load (variable resistor). Q1 and Q2 are IGBTs of IRGP4062D type. The circuit was chosen to verify the main goals of the gate driver performance which are the following:

- Gate driver desaturation protection performance,
- Gate driver high switching capabilities,
- Gate driver PCB performance.

6.5 Experimental results

The test was conducted at low voltage and at different frequencies and different load values. The recorded values were done at 5 kHz switching frequency, 50% duty cycle with 2 μs dead time and 20 - 30 V DC power supply. The DC power supply was fixed in the range of 20 to 30 V DC in order to visualize the behavior of the gate driver desaturation protection at no load and at low supply voltage.



a)

b)

c)

d)

Figure 6.5: Behaviour of an IGBT gate driver power supply

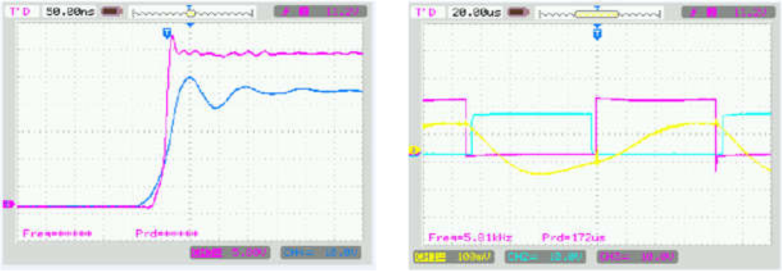
Two boundaries for the gate drive operation were analyzed during this experimental work. In addition, the consumption at each level of the power supplied was experimentally calculated. The frequency was set at 5 kHz in order to visualize the behavior of the power consumption. Fig. 6.5 shows the output current and voltage at different capacitor values (Fig. 6.5 a), the input and output voltage when the supply is lightly loaded with 1 kΩ resistor and when the supply is loaded with 10 kΩ resistor are shown in (Fig. 6.5 b) and (Fig. 6.5 c), respectively. Loading the gate drive power supply from 1 kΩ to 10 kΩ showed the critical operation point of the gate driver. At these points, the under-voltage lockout (ULVO) and the desaturation protection must be active. Loading the gate driver power supply by 10 Ω indicated the transformer draws 0.26 mA at 100 kHz and the total consumption was 15 mA [Fig. 6.5.d]. The characteristics of the power supply of the gate driver permitted to test the remaining part of the IGBT gate driver.

A. Gate switching capability

The gate driver has fast switching ON and OFF capability because the gate resistor is very small, 1.5 Ohms. Fig. 6.5 a) shows an unloaded switching delay time, td is 4 ns with voltage overshoot of 4 V. Therefore, the related switching losses are very low. Similarly, the switching losses at high voltage can be estimated very low as well since the key factor that influences the losses is the switching delay time. The losses during standby state of the gate driver was measured. And it turned out to be 0.75 mA.

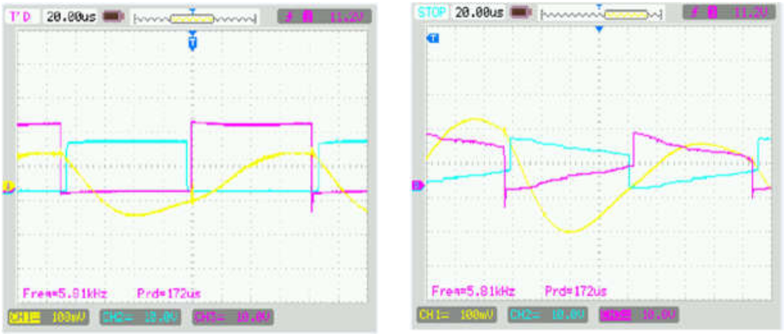
B. Gate driver desaturation performance test

At normal operation, the voltage across R7 is 0.5 V. The more the inverter is loaded the more the R7 voltage decreases. Fig. 6.5 show the gate driver operation dynamic behavior. In Fig. 6.5 , the turn ON transient time is observed. Fig. 6.5 shows that during desaturation phenomenon, Q10 shorts circuit the power supply. During the transient time of the desaturation protection, the gate voltage is pulled down [Fig. 6.5.d)]. Once the current keeps on increasing, Q10 cuts off the power supply and gate driver signal collapses. The Fig. 6.5 d) shows that at R7= 8.2 kΩ the desaturation protect reacts at 10 A . This current desaturation drops at 7A while R7=6.2 kΩ. This can be observed as well at the level of the power supply. Once the current desaturation value is reached, the power supply pulls down the voltage. It helps to switch OFF the IGBTs slowly compared to the switching speed during the normal operation, by pulling down the internal supply. This avoids the high voltage spikes.



a) IGBT,Q1, gate voltage (blue) and Output voltage (Purple) at 5 kHz

b) Q2 Gate-emitter voltage (blue) ,Q1 Collector-emitter voltage(purple) and current (yellow) at 5 kHz before the desaturation protection



c) Q2Gate-emitter voltage (blue) ,Q1 Collector-emitter voltage(purple) and current (yellow) at 5 kHz before the desaturation protection

d) Voltage output (purple), Q1 Gate emitter voltage (blue) output current (yellow) at desaturation protection level while driving the IGBTs at 5 kHz

Figure 6.5: Experiment results

6.6 Conclusions

Several features could be implemented in the gate drive. The actually used gate drivers inject a non-negligible capacitive current in the mass of the control circuit. The solution proposed by the paper is to use very cost effective and less parasitic capacitance inductive components, sold as common choke filters, so that each transistor can use its own supply. The low parasitic capacitance reduces the typical EMC problems in power electronic driving circuits [16]. The gate driver has a desaturation protection feature, which can be detected at level of power supply. The results shows that the gate driver has a very low total parasitic capacitance of order of 4 pF. A second feature is a very low stand by consumption. A third feature is a gate driver circuit design without electrolytic capacitors, which is desired for a longer converter life. A fourth feature is that desaturation protection could be obtained while still using an 8-pin driver IC. The tests shows it can protect a short circuit within a few μs. The gate driver is adjustable by hardware type, making it independent from software or current sensor problems. Finally, the gate drive is tested but not implemented in the final converter of the next chapter, as another set-up has been used due to the limited available time in the project. But independent from the used set-up, this type of gate drive could improve also other converter types.

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Chapter 7

Experimental test of the proposed topology

7.1 Introduction

Different parts of the proposed topology have been tested. Chapter 4 tested the behaviour of DC-link by simulation and experimental work whereas chapter 6 presented a design and a hardware implementation of the gate drive that can be used for the proposed topology. Yet, an experimental test of the entire proposed topology is needed. The main aim of the PhD was to see if a modulated DC-link was possible, unfortunately the total cumulated stay of 22 months (Rwanda was counted for experimental work) in

Gent before submission was too short to have a thourough testing at full voltage and current. In fact, this chapter presents the tests related to the current control and to the modulation techniques. However, the test at full voltage and full current was not reached.

7.2 Experimental set up

The proposed topology can be applied to any three-phase topology with slight change of hardware. However, selecting the convenient switches is necessary and a correct small DC-link film capacitor. The current control algorithm was verified using the three phase inverter set up of the INCREASE project [1]. The developed prototype has a three phase inverter that has individual IGBTs [1]. IGBts used are IXYB82N120C3H1. A slight modification was made based on Fig. 7.1. In fact, the following components and their values were considered for the performance of the proposed topology [2].

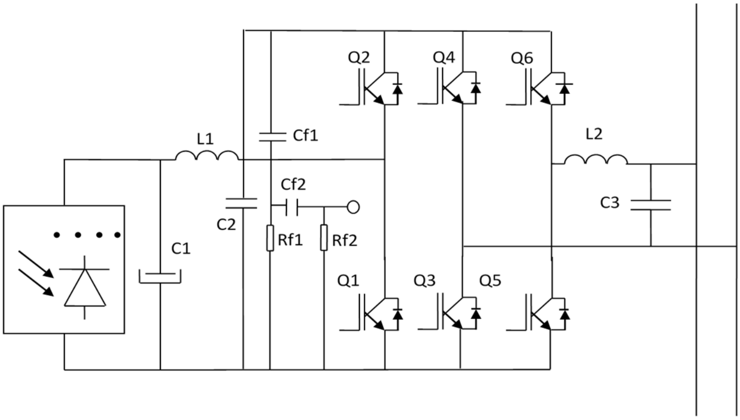


Figure 7.1: Single phase grid connected circuit

C1, an electrolytic capacitor, has a large value of 2200 µF, C2 and C3 are propylene film capacitors and their values are 20 µF, and 10 µF respectively. Cf1, Cf2, Rf1 and Rf2 constitute a high pass filter. Cf1 and Cf2 are respectively 10 nF and 1 nF. Rf1 and Rf2 are respectively 5 kΩ and 50 kΩ. The sizing and the tuning of the high pass filter are explained in chapter 4 of this book and in the published paper related to this work [3]. Fig. 7.2 shows a slight change made on the mentioned set up. The red capacitors are parts of the high pass filter. The four blue capacitors in parallel compose C2. Each capacitor is 5 uF. From the calculation based on the acceptable ripple, L2 is 1400 uH and L1 is 700 uH. L2 becomes bigger than L1 because C3 is smaller than C1. Since the step up can operate in a boost converter mode while the grid voltage is lower than the DC-link voltage, an overvoltage protection is required. A protection circuit avoids having transistors destroyed, in case the loop would not function well or if a processor hangs.

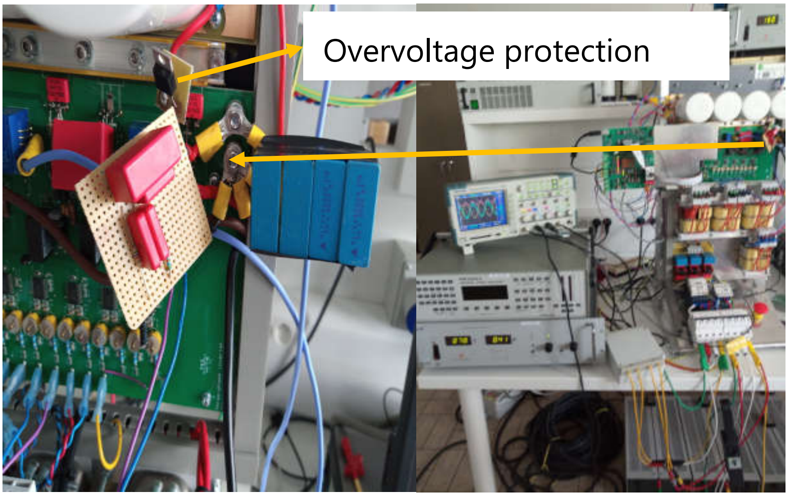


Figure 7.2: High pass filter (HPF) and a DC-link capacitor

This can stop all signals to the transistors to shut down the system when the DC voltage becomes higher than the maximum rated value. An overvoltage could have many other reasons as well. or an induced voltage by lightning, a startup of a medium voltage transformer, a current protection by a fuse or circuit breaker. An overvoltage protectioncircuit based on a zener diode was included to the set up [Fig. 7.2]. The same protection was published in the paper related to this work [2], so it has been tested in an earlier stage.

Table 7.1: Estimated current ripples while L1=700 µH, L2=1400 µH, switching frequency is 25 kHz

V_{DC}	**Vgrid**	**Duty cycle for both DC and H inverters**	**I_{ripple}**
100 V	100 V	100%	4.2 A
200 V	100 V	50%	2.86 A
200 V	100 V	25%	2.8 A

Table 7.2: Estimated voltage ripples across C2 while C1=4400 µF, C2=20 µF, switching frequency is 25 kHz

V_{DC}	**Vgrid**	**Duty cycle for both DC and H inverters**	**V_{ripple}**
100 V	100 V	100%	45 V
200 V	100 V	30%	20 V
200 V	100 V	25%	10.85 V

The used passive components are calculated for a 3 kW single phase inverter. Based on the power of the proposed inverter, Table 7.1 and Table 7.2 give the image of estimated current and voltage ripples for different scenarios that the experimental work is based on to verfy the concept. For both tables the voltage and current ripple are acceptable. However, the issues becomes while the duty ratios for the DC converter and the H-bridge are equal to a unit. The system can present a resonance phenomenon originated between L1, L2 and C2. This requires a fast control. The right feedback and feed forward control might be needed. The practical experiment had to take this into consideration. The used step up has an inductor of 300 uH. This is not considered as a problem for the proposed topology as at that place it is less relevant for EMC. Figure 7.3 explains the control block diagram of the duty ratios based on the inductor current, IL2. I_{set} is grid current reference value. The PLL is used to compute a synchronous sine wave value that is later scaled by a MPPT to form a reference current. The PI is used to correct the error. The error is added with a portion of the high pass filter output in order to give the controlling function, Fc. To better and easy tune the PI parameters, an RC circuit (10µF and 5 ohm) was initially connected in parallel with C2, it permits to start from a stable situation and gradually tune the system.

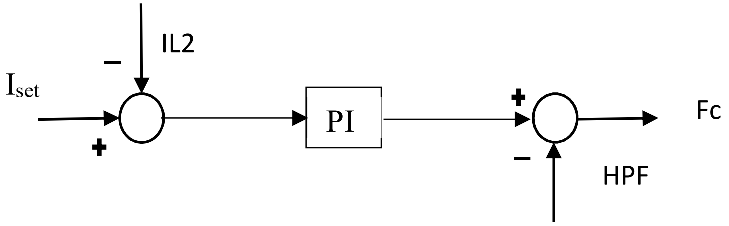
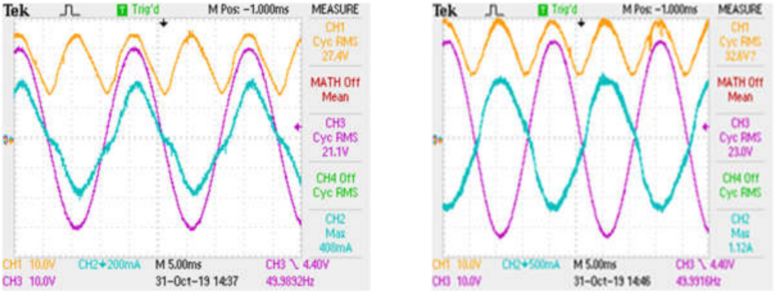


Figure 7.3: Control block diagram

In fact, this was learned from simulations. The initial value of PI were obtained in the fourth chapter of this book. The constants of PI were kept constant and the values of the RC circuit components were reduced until the instability of the system is obtained. From the state of the instability, the PI were retuned for reaching the new stability state of the system. At the end the stability of the system was reached while the values of the RC circuit components were null. Similar to what has been done in simulation, Fc helps the system to operate in the required modes, boost or buck converter mode (first leg), or H-bridge. The Texas instrument, TMS320F2833S, was used to process signals. The codes were written in Code Composer Studio 6.1.

7.3 Experimental results

The experiment shows the behaviour of the three signals. The first signal is the DC voltage. On Fig. 7.4, the DC-link voltage (orange signal) is modulate following the theory discussed in chapter 3. It is obvious that the two operation modes are active. Once the grid voltage is positive (purple signal), H-bridge reacts as buck converter. While the grid voltage sign is negative, the boost converter acts. Consequently, the C2 does not experience high voltage ripple changes. In fact, the switching in Q5 and Q6 is limited since on the top of the grid voltage do not switch. A scale test is made at lower voltage and lower current to get still similar impedances.

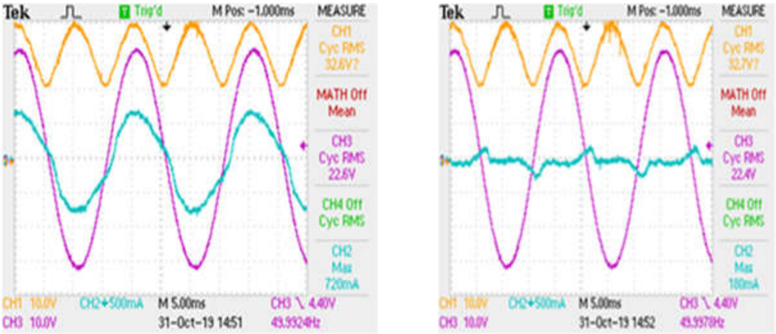


a) b)

Figure 7.4: Purple: Grid voltage. Blue: inductor current

Yellow: DC link voltage

a) Grid supplies the inverter , b) Grid is supplied by the inverter

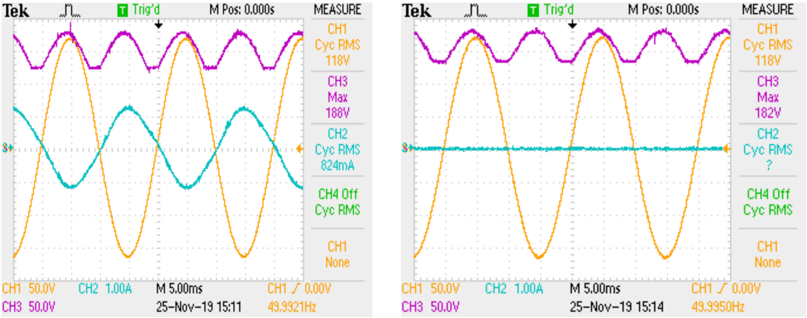


a) b)

Figure 7.5:

a) Inverter supplying
b) Different between injection current to the grid and absorbed current from the grid

On Fig. 7.4.a, the current is quite in phase with the grid and injects power to the grid. It is operating close to the unity power factor. Fig. 7.4.b, the inverter is operating as a load.



a) b)

Figure 7.6:

a) Voltage waveforms while a load is connected to the inverter

b) Voltage waveforms while the inverter is at no load

Hence, it is supplied by the grid. Note that the case b) shows that the same converter could operate to charge for example a battery positioned at the input instead of a PV array, using the same topology. This similar to the functionality of the topology in [4]. The reverse energy flow mode is anyhow needed even in the inverter mode, if the power factor is not unity and hence some energy has to flow back to C1 in a minor part of the period [5]. Fig. 7.5 shows the behaviour of the current while supplying 2 A peak and it presents the difference in current between the injection current to the grid and consumption of the current from the grid. In other words, the shows the harmonics injection of the inverter to the grid. The previous results were obtained at low voltage. The objectives of the experiment was to taste the stability of the proposed alogorthm. A test with a higher voltage was conducted in order to visualize the behaviour of the control at a voltage value closer to practical voltage. Fistly, the inverter was supplied by 100 V_{DC} from a PV emulator and connected to a grid emulator of 100 Vac. A load of 100 Ω was connected to the inverter. Fig. 7.6 shows the DC-link voltage (purple), the grid voltage (orange), and the load current(blue). At no load , Fig. 7.6 a, power loss of 70 mW is observed. This is the consumption of the inverter at no load. At a load of 100 Ω, 97.2 Watts is consumed.

7.4 Conclusions

After testing the proposed topology using a standard three-phase inverter topology originally developed for INCREASE project, but where the DC-link has been adapted, the experiment showed good results and proofs that a modulation of DC-link can be used with an appropriate feedback methodology. In this way, PWM modulation of the H-bridge at the top of the sine of the grid voltage could be avoided. In this way a converter with only one electrolytic capacitor at a non-critical place at the input can be achieved.

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Chapter 8

Conclusion and Future of Works

8.1 Conclusions

In this thesis, the issue of the use of renewable energy in Rwanda has been discussed. The thesis has shown the drawbacks of using electrolytic capacitors in the DC-link of a single-phase inverter. From the drawbacks of the classical single-phase inverter topology, the new topology with a propylene film capacitor in the DC-link has been proposed and tested. It has been shown that the proposed topology can use a standard three-phase transistor bridge for a single-phase grid connected inverter. The inverter needs a specific voltage modulation and feedback. The middle leg plays a role of quadratic selection. The first leg is in charge of stepping up or down the voltage depending on the level of DC voltage. The inverter is low current ripple type since it has the input inductor L1 and the output inductor, L2. The advantage of using inductors at input and output combined with limited voltage levels is that low current ripples are obtained. Placing the electrolytic capacitor at the input and propylene film capacitors at DC-link reduces the current RMS value in inductors compared to the usual single-phase inverter. The RMS current in the DC-link capacitor is also lower. Consequently, the losses can be reduced. By Matalab simulation, the proposed topology presents a good performance in terms of stability, and would have less ripple injection in the grid for the same inductors.

The main contributions of the thesis are summarized in the following points.

- A stability analysis of the DC-link of the proposed topology. In Chapter 4, the thesis shows that the proposed PV inverter topology will react in a damped way to a disturbance from the grid. A small capacitor at the DC-link is necessary for enough bandwidth but can impair the stability. Therefore, a tool of testing the stability of the DC-DC part has been employed. The test of the DC-DC part stability of the proposed topology has been conducted using mainly Numerical Inverse Laplace Transform. The results of this technique have been helpful to tune the control parameters of a PV buck boost converter. A way to introduce damping is creating an active damping similar to a damping resistor at the DC-link level. A PWM with high pass filter feedback on the

DC-link has been used to proof check the stability of DC-DC link of the proposed topology, the conclusion is that a feedback of the DC-link voltage improves the damping to a sufficient level. The next analysis can be extend to the H-bridge part of the topology. The chapter five focuses more on this concern.

- Frequency synchronization using the double integration method (DIM). Chapter 5 has shown that A double integration synchronization method (DISM) is an alternative synchronization method for a DC/AC grid tied frequency. The chapter presents how the integrator initial_constant can be removed in order not to deteriorate the input signal. It delivers useful signals from the first period. The DISM is simpler to program and to simulate than a PLL. The behaviour is easier to predict, as PLL systems are depending how the synchronisation happens and how software goes from fast synchronisation to a slower feedback to be more insensitive to harmonics. Some simulations and lab experiments that can be applied on real system are presented in this chapter to show the dynamic performance of the DISM. It could be used to help a fast start of the grid after a shutdown.
- Design consideration of an IGBT gate driver. After showing that the actually used gate drivers inject a non-negligible d*V*/d*t* slope induced capacitive current in the mass of the control circuit, Chapter 6 has shown four features of the proposed gate driver. The solution proposed by the thesis is to use very cost effective and less parasitic capacitance inductive components, sold as common choke filters, so that

each transistor can use its own supply. The low parasitic capacitance reduces the typical EMC problems in power electronic driving circuits. It can be realised without any electrolytic capacitor. The thesis has shown that the gate driver has a desaturation protection feature, which can be detected at level of power supply. The results have shown that the designed gate driver has a very low total parasitic capacitance of order of 4 pF. A second feature of the gate driver is that it has a very low stand by consumption. A third feature is a gate driver circuit design without electrolytic capacitors, which is desired for a longer converter life. The fourth feature is that desaturation protection could be obtained while still using an 8-pin driver IC. The tests shows it can protect a short circuit within a few µs. The gate driver is adjustable by hardware type, making it independent from software or current sensor problems. Finally, the gate drive is tested but not implemented in the final converter of the next chapter, as another set-up has been used due to the limited available time in the project. But, independent from the used set-up, this type of gate drive could improve also other converter types.

8.2 Future works

Although the work presented in this thesis has achieved some interesting results related to the proposed single phase topology many problems remain open and will be the subject of future investigations. The main future research items are:

- Use automotive grade components and processors that are designed and tested for a wide temperature and humidity range for a single-phase inverter.
- Improve the protection so that an inverter can resist to indirect or direct lightning flashes.

List of scientific publications during my PhD

1. Articles published in international journals

[1] **Bikorimana Jean Marie Vianney**, Mohannad Jabbar mnati, and Alex Van den Bossche."Frequency Synchronization of a Single-phase Grid-connected DC/AC Inverter Using a Double Integration Method."Automatika, vol.58, no.2, pp.141-146, 2017.

[2] **Bikorimana Jean Marie Vianney**, and Alex Van den Bossche "Less-conventional low-consumption galvanic separated MOSFET-IGBT gate drive supply" Hindawi Active and Passive Electronic Components Volume 2017, Article ID 4181549.

2. Publications in the proceeding of international conferences

[1] **Bikorimana Jean Marie Vianney**, and Alex Van den Bossche." Low Parasitic Capacitance Gate Driver with Desaturation Protection". International Conference on Mechanical Materials and Renewable Energy, 2nd, 2019.

[2] **Bikorimana Jean Marie Vianney**, and Alex Van den Bossche "Direct DC use of PV for cooking and sanitary". International Conference on Mechanical Materials and Renewable Energy, 2nd, 2019.

[3] Mohannad Jabbar Mnati Al-Rubaye, Alex Van den Bossche and **Jean Marie Vianney Bikorimana**." Design of a half-bridge bootstrap circuit for grid inverter application controlled by Pic24fj128ga010". International Conference on Renewable Energy Research and Applications, 5th, 2016.

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[5] **Bikorimana Jean Marie Vianney**, and Alex Van den Bossche "Euro-African business partnership on the forefront: opportunities and challenges with case study of Photovoltaic converter business". Gent Africa Platform Symposium, 9th, 2015.

[6] **Bikorimana Jean Marie Vianney**, and Alex Van den Bossche "Using numerical inverse Laplace for optimizing the current control in grid coupled inverters". International Conference on Electro-Energy, Proceedings, 2014

[7] **Bikorimana Jean Marie Vianney**, and Alex Van den Bossche "Using numerical inverse Laplace for

optimizing the current control in grid coupled inverters”. International Conference on Electro-Energy, Proceedings, 2014

[8] Alex Van den Bossche, **Jean Marie Vianney Bikorimana**, and Firgan Nihatov Feradov” Reduced losses in PV converters by modulation of the DC link voltage”. International Conference on Renewable Energies and Power Quality, 14th, 2014